LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
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Technical Note	**LIGO-E050262**	01/19/10

Test procedure for the Timing Slave Board Advanced LIGO

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This is an internal working note
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Board document LIGO DCC # 070071

Board **Revision C**

Board Serial #

Board Type **Slave**

RoHS complient ☐

Test Engineer

Test Date:

Overall Slave board testing: **PASSED** ☐ **FAILED** ☐

The following Test Procedure describes the test of proper operation of the Timing Slave board (LIGO-D070071, thereafter, Slave). Slaves provide 1PPS/UTC synchronous timing and diagnostic signals to external devices that are needed to be synchronized in different, possibly distant parts of the detector. The Slave receives 1PPS/UTC synchronous timing signal from Fanout/Master upstream[1] (LIGO-D070011) that it synchronizes to.

Required test tools and equipment:

- *Two DC Power Supplies (1. +12V, 1A or more, with current readout – use BLZ 5.08/2 connector to supply power to Slave Board, 2. +24V, 1A or more for the Master)*
- *Slave Board (D070071)*
- *Timing Master (LIGO-D070011 & LIGO-D080094)*
- *2xLC optical fiber, with SFP Transceiver modules(e.g. HFBR-57E0PZ) on both ends*
- *Altium USB JTAG Adapter*
- *Computer with working versions of Altium Designer and Xilinx ISE WEbPack.*
- *Voltmeter with test leads*
- *Oscilloscope - 500 MHz (if it has no 50Ohm termination option, a BNC T and a 50Ohm terminator is also needed)*
- *Test Daughterboard (D080192 rev B)*
- *BNC cable*
- *Home-made test board for testing the leads of P3 connector on the Slave board*

In the Test Procedure, one will need to use a Test Daughterboard (LIGO-D080192) that will be attached to the Slave to facilitate the test of its connectors. At the start of the Test Procedure, the

[1] In some cases, the *Slave* board might be directly connected to the *Master*, or there might be several boards serially connected between the *Master* and the *Slave*.

Test Daughterboard should NOT be attached to the Slave. In the Test Procedure, ground will be denoted with GND. ***Measured voltages on the Slave or Test Daughterboard should be referenced to GND, which is available on test points TP9 and TP10 on the Slave (Figure 1) and TP1 on the Test Daughterboard.***

1) Verify the proper current draw. Using a bench DC power supply apply +12V to the *Slave*. Connect +12V to port 1 of the SL 5.08/2 screw terminal (P7, figure 1) and GND to port. Measure the current draw of the board. Check if the power LED (DS3, figure 1) is ON after you apply the voltage.

+12V at < 430 mA Measured mA ☐Pass ☐Fail

Power LED is on ☐Yes ☐No

2) Verify that the power supply rails are at the correct voltages. Measure the voltages at the following test points (for test point locations please refer to figure 1). **If any of these indicators of proper operation are not present the problem must be fixed before proceeding with the test.**

TP8 (12V), +12V (11.4 – 12.6)V ☐Pass ☐ Fail

TP4 (VDD), +3.3V (3.14-3.46)V ☐Pass ☐ Fail

TP5 (AUX), +2.5V (2.38-2.62)V ☐Pass ☐ Fail

TP3 (INT), +1.2V (1.08-1.32)V ☐Pass ☐ Fail

TP6 (Conf), +1.8V (1.62-1.98)V ☐Pass ☐ Fail

TP7 (P10V), +10V (9.5-10.5)V ☐Pass ☐ Fail

3) Check if the JTAG connector works properly.
- Connect the JTAG Interface (figure 2) to the JTAG connector (figure 1) of the *Slave*.
- Program the *Slave* with the *FGPA_SLAVE_TEST* program. (See Appendix)
- In the Altium Designer program, open the digital I/O unit called U_Test (see figure A2 in the Appendix). At the upper left corner of the window, the JTAG variable is should be 1/0 if the program has loaded properly (figure 3).

JTAG connector works properly. ☐Yes ☐ No

For the following tests one also needs a working complete (chassis integrated) Master timing module (LIGO-E090002), with FPGA_MFO program loaded onto the board via a JTAG adapter connecting to the rear panel of the chassis.

The FGPA_SLAVE_TEST program should be loaded onto the Slave board (see Appendix for FPGA program instruction). During the test, you will be asked to connect the Slave board to a Master board with a 2xLC optical fiber. The optical fiber should be connected to the SYNCIN connector (J1) of the Slave (Figure 1) through an SFP Transceiver module with optical 2xLC connector. The other end of the fiber should be connected to one of the 1-16 output s of the Master/ also through an SFP Transceiver module (figure 4). This transceiver module is removable and should be placed in the SFP connector of the board.

4) Verify the proper operation of HF PLL (phase lock loop).

a. Using a Voltmeter, measure the voltage on the Control Mon output TP2 (CTRL) (figure 1). With no SYNCIN signal, the control voltage should be at the negative rail, which is 0V, indicating that the loop is unconnected. The 1PPSIN LED (DS1 on figure 1) should be off.

b. Next, connect the optical fiber with one of the SYNCOUT signals from the *Master* (labeled 1 to 16 on the front panel of the Master chassis, figure 4) to the SYNCIN connector of the Slave (J1, figure 1).
First, the 1PPSIN LED (DS1) should be ON for 250 ms (quarter of a second) and OFF for the next 250ms, indicating that the board receives the SYNCIN signal, but it is not locked to the (or *Master*) yet. After locking, the LED will be ON for one second and OFF for the next.
For this part of the Test, exhibiting *quarter second and 1 second blinks* are both acceptable.

c. If HF PLL is locked, the control voltage will no longer be railed and should be roughly 5V. Record the locked control voltage.

d. Also check if the power draw of the *Slave* has changed significantly due to the connection of the optical fiber (a significant change shows improper operation - some components are probably shorted).

a. TP2 (disconnected fiber) at 0V ± 0.1V	Measured	V	☐Pass	☐Fail
b. 1PPSIN LED works properly (blinks)			☐Yes	☐No
c. TP2 (locked, connected fiber) at 5V ± 1V	Measured	V	☐Pass	☐Fail
d. Current Draw for board at < 430 mA	Measured	mA	☐Pass	☐Fail

5) Write down the value of the VCXO Control ADC and compare with the analog readback. In the Altium Designer program, open the digital I/O unit called U_Test (see figure A2 in the Appendix) for the *FGPA_SLAVE_TEST* program. Compare the value of the variable VCXO_CONTROL[15..0] (shown as e.g. 03-1773 on figure 4) with the Control Mon output TP2 (CTRL) on the *Slave*. The value of VCXO_CONTROL[15..0] can be converted to Volts with the following formula:

$$V\_OCXO\ [V] = VCXO\_CONTROL[15..0]\ /\ 6553.6$$

(For example 03-1773 on figure 4 converts to 31,773/6553.6 = 4.85 Volts.)

If the ADC works properly, V_VCXO and TP2 should be roughly equal, within ±0.1V of measured values at TP2 in test 4) above. Verify for the cases of connected and disconnected optical fiber separately.

V_VCXO (connected fiber) Measured V

V_VCXO (disconnected fiber) Measured V

These voltages are within ±0.1V of that measured in test 4) at TP2 and thus the ADC works properly: ☐Yes ☐No

6) Verify the synchronization of the 1PPS (pulse per second) signal.
- Connect the 1PPS OUT output of the Master, located at the rear panel of the Master chassis, to an oscilloscope using a BNC cable and 50 Ohm termination.
- Also connect pins 15 (SYNCLK_P - signal), and 16 (SYNCLK_N - GND) of the P3 header of the *Slave* to a second channel on the oscilloscope using 50 Ohm termination.
- Trigger on the signal from the *Master*.

-Each monitor output should be putting out a positive going, 10μs wide 1PPS signal.
-The 1PPS signal from the *Slave* should be properly synchronized, i.e. its leading edge should match the leading edge of the 1PPS signal from the *Master* within **± 60ns** (see figure 5).
-The synchronization should disappear when the link between them is disconnected.
-If the 1PPS signals are synchronized, the SYNCOUT LED on the *Master* (one of the green LEDs, labeled 1-16 on the front panel of the Master/ chassis, corresponding to the given output in use) and the and SYNCIN LED (DS1) on the *Slave* (figure 1) should *blink* with a rate of 1 sec on, 1 sec off. If the 1PPS signal is not synchronized but the boards are connected, the LEDs on both would *blink* significantly faster, with quarter sec on, quarter second off. If there is no 1PPS signal present, but the boards are connected, the LED is constantly ON.

$|\Delta t|$ (1PPS OUT (Master/) – SYNCLK_P (Slave)) ns

DS1 on the *Slave blink*s slower with a rate of 1s on - 1 s off ☐Yes ☐No

Master and Slave 1PPS signals are synchronized. ☐Pass ☐Fail

7) Test the P3 header of the *Slave*.

For this test it is suggested to prepare a home-made test board that allows easy testing of the pins on the P3 header of the Slave.
Pins 1-8, 10, 12 and 14 should be tested with a Voltmeter. Their outputs should be the following:

2, 4, 6, 8, 10, 12, 14:	GND
1, 3:	+12V (11.4 – 12.6)V
5, 7:	+3.3V (3.14-3.46)V

Measure pin 9 with an Ohmmeter. It should be toggling between shorted and non-conducting states each second (grounded for a second and then non-conducting for the next second). In 5) pins 15 and 16 were already tested.

Pins 2, 4, 6, 8, 12, 14	☐Pass	☐Fail
Pin 1	☐Pass	☐Fail
Pin 3	☐Pass	☐Fail
Pin 5	☐Pass	☐Fail
Pin 7	☐Pass	☐Fail
Pin 9 is toggling between shorted and non-conducting states	☐Yes	☐No
P3 header on the Slave works properly	☐Pass	☐Fail

For the following tests, the Test Daughterboard (D080192 Rev B) should be placed onto the Slave board. First turn off the 12VDC power to the Slave board. Place the Test Daughterboard onto the Slave board and make sure that it is seated properly (figure 6). After turning on the power for the Slave board verify that the FPGA_SLAVE_TEST program is loaded on the board (see Appendix).

8) Test the SN(P)[64..1] ports on the *Slave* board.
In the *FGPA_SLAVE_TEST* program, every even port (i.e. S2, S4, etc.) is output, while every odd port is input. The outputs are all HIGH for one second and then LOW for the next second. The *Test Daughterboard* connects the even ports to the odd ports: even port S[2n] is connected to odd port S[2n-1].
In the Altium Designer program, open the digital I/O unit called U_Test (see figure A2 in the Appendix) for the *FGPA_SLAVE_TEST* program. The states of the SN(P)[64..1] ports are shown by LEDs:

SN(P)[16..1] => SN(P)_A[16..1],
SN(P)[32..17] => SN(P)_B[16..1],
SN(P)[48..33] => SN(P)_C[16..1],
SN(P)[64..49] => SN(P)_D[16..1].

If the *Test Daughterboard* and the ports work properly, all soft LEDs should exhibit a *blink* with – 1 sec on, 1 sec off. (Note that sometimes it is difficult to properly place the *Test Daughterboard*, therefore it might not connect all 64 ports properly. If some of the ports do not connect, try to re-seat the *Test Daughterboard* before concluding that some ports do not work.)

Are there any SN(P) ports that do NOT blink (1 s on, 1 s off)? ☐Yes ☐No

If yes, specify the faulty ports (e.g. SP49)

Try reseating the board one again. Is there still a problem? ☐N/A ☐Yes ☐No

All SN(P)[64..1] ports work properly ☐Pass ☐Fail

9) Test the DIP-8 socket on the *Test Daughterboard* with a voltmeter. The DIP-8 socket is shown on figure 5. Test each pin except pin 2 with a Voltmeter. Use TP1 on the Test Daughterboard for GND. Their outputs should be the following:

1, 5, 6 toggling: HIGH (~2.5V) for a second and then LOW (~0V) for the next second
3, 7, 8: HIGH (2.5V, (2.38-2.62)V)
4: LOW (0±0.1)V

Check if the input pin, pin 2, works properly. Turn on the U_Test digital I/O in the Altium Designer. The soft LED called CFG_SI (see figure 3) should be OFF since there is no input. Now connect pin 2 with pin 1: CFG_SI should *blink* with 1s on, 1s off.

Check mark pin if toggling (1 sec on, 1 sec off) is observed: ☐Pin 1 ☐Pin 5 ☐Pin 6

Pin 3 ☐ Pass ☐Fail

Pin 4 ☐ Pass ☐Fail

Pin 7 ☐ Pass ☐Fail

Pin 8 ☐ Pass ☐Fail

Pin 2 works properly ☐Yes ☐No

DIP-8 socket works properly ☐Yes ☐No

10) Test switches 1 to 8 on the *Slave* and switches 1 and 2 on the *Test Daughterboard.*

In the Altium Designer program, open the digital I/O unit called U_Test (see figure A2 in the Appendix) for the *FGPA_SLAVE_TEST* program. In the program SW[10..1] gives the SW inputs.
- SW[8..1] represent the switches located on the *Slave* (S2 on figure 1).
- SW9 and SW10 correspond to Switch1 and Switch2, respectively, on the *Test Daughterboard*.

If SW9 and SW10 are not pressed, the corresponding values in the digital I/O should be HIGH. If the switches are pressed, these values should go LOW as long as the switches are pressed.
-The values of SW[8..1] can be set manually with the S2 unit on the *Slave*. On S2 you find eight switches that can set the values of these switches to HIGH or LOW. Test if these switches induce the desired changes in the SW[8..1] values as seen on the digital I/O unit. Note that, if these switches have not been used before, they have a thin safety cover on them that has to be broken in order to be able to use the switches.

Check mark the switch if proper operation is observed:
☐ SW1 ☐ SW2 ☐ SW3 ☐ SW4 ☐ SW5 ☐ SW6 ☐ SW7 ☐ SW8 ☐ SW9 ☐ SW10

Switches 1 to 8 on the *Slave* work properly ☐ Yes ☐ No

Switches 1 and 2 on the *Test Daughterboard* work properly ☐ Yes ☐ No

11) After test procedure the following needs to be verified for having the board ready for shipment

1. If the board passed this test, turn off power to the board and disconnect incoming cables. Disconnect the Test Daughterboard. Assign a serial number and add a serial number sticker to the board and save this document with the following name: TestD70071#serial.pdf
   Print 3 additional serial number stickers for future purpose.
2. Save the additional test documents if available (e.g. FPGA X-ray image as FPGA_XrayD70071#serial.pdf)
3. Turn on the power again and program the Slave Board with the corresponding program for installation. (e.g. if the Slave will be used with DuoTone DaughterBoard, program with the DuoTone FPGA code: Timing/FPGA/DuoTone/ProjectOutputs/Spartan3/fpgaduotone.mcs)
4. Turn off power. Disconnect all cables. Attach the heatsink to the FPGA (INM19001-23W/2.6BU)
5. Place a BLZ 5.08/2 connector into P7.
6. Switches 1-8 on S2 of Slave board should be left in OFF position.

7. Attach the appropriate Daughterboard if available (e.g. DuoTone board) using the required mechanical parts (standoffs, screws) and prepare for testing e.g. the Slave/DuoTone functionality.

Notes:

FIGURES

Figure 1

Locations of testpoints (TP) and other connector elements on D070071

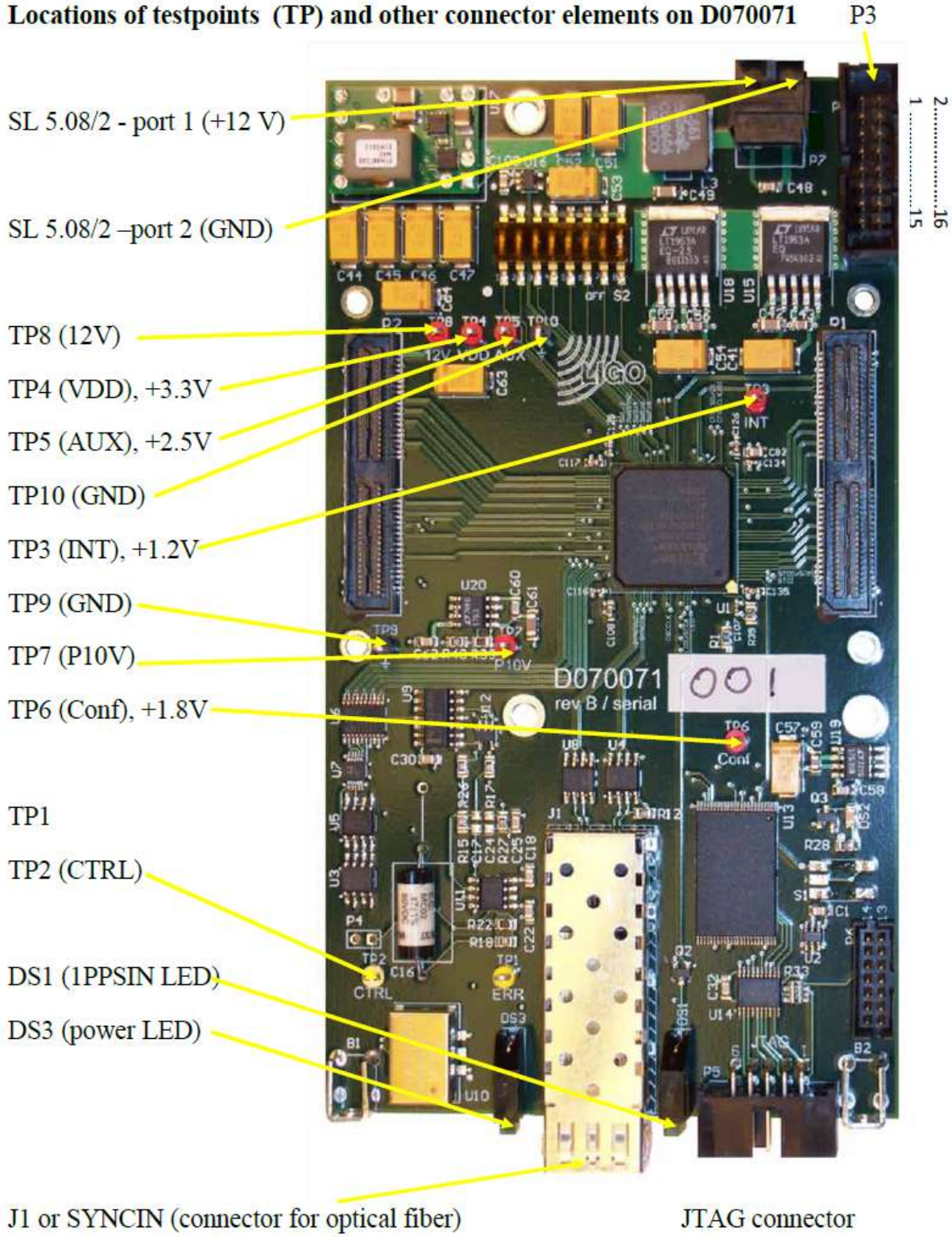


Figure 2 JTAG Interface
Note: The JTAG Interface needs to connect to a laptop/computer via a USB (for power) and the other end connects to the JTAG connector on the Slave board (P5)

Figure 3 Screenshot for the Digital I/O unit, U-Test
-The JTAG variable is at the upper left corner.
- VCXO control [15…0] is the 11th line
- SP and SN ports are lines 1-8 (Note that SP_D[1] i.e. SP49 is not working properly in this test.)
-CFG_SI LED is on line 9.
-SW[10..1] switches – line 10.

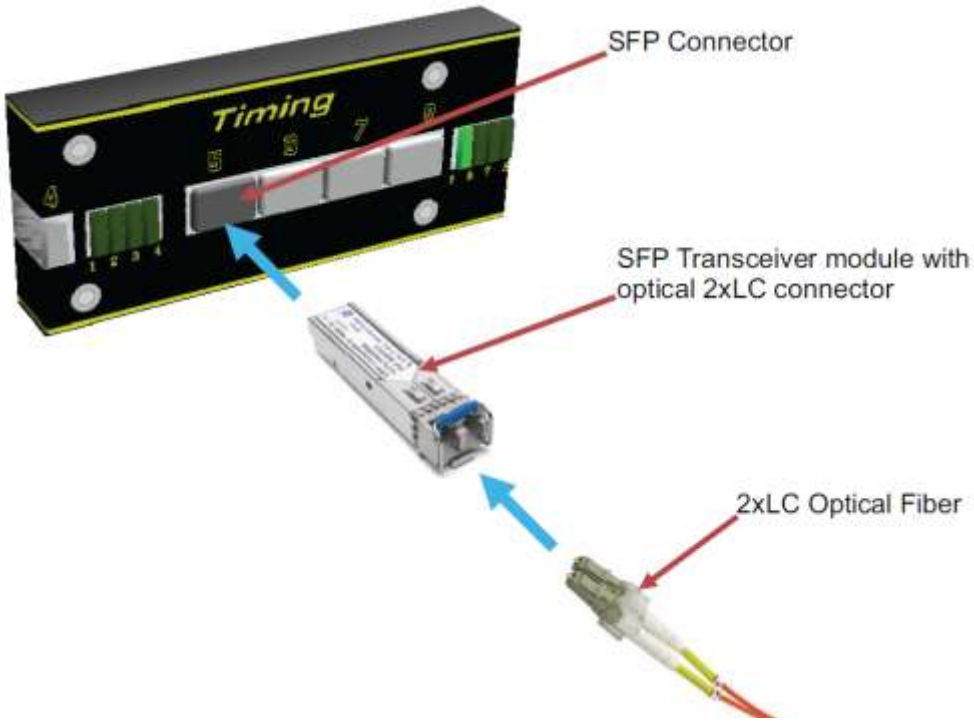


Figure 4 Connection of 2xLC Optical fiber to an output on the Master/

Figure 5 Screenshot from oscilloscope: top trace (Ch1): Master, bottom Trace (Ch2): Slave 20 ns/div is used on the horizontal axis.

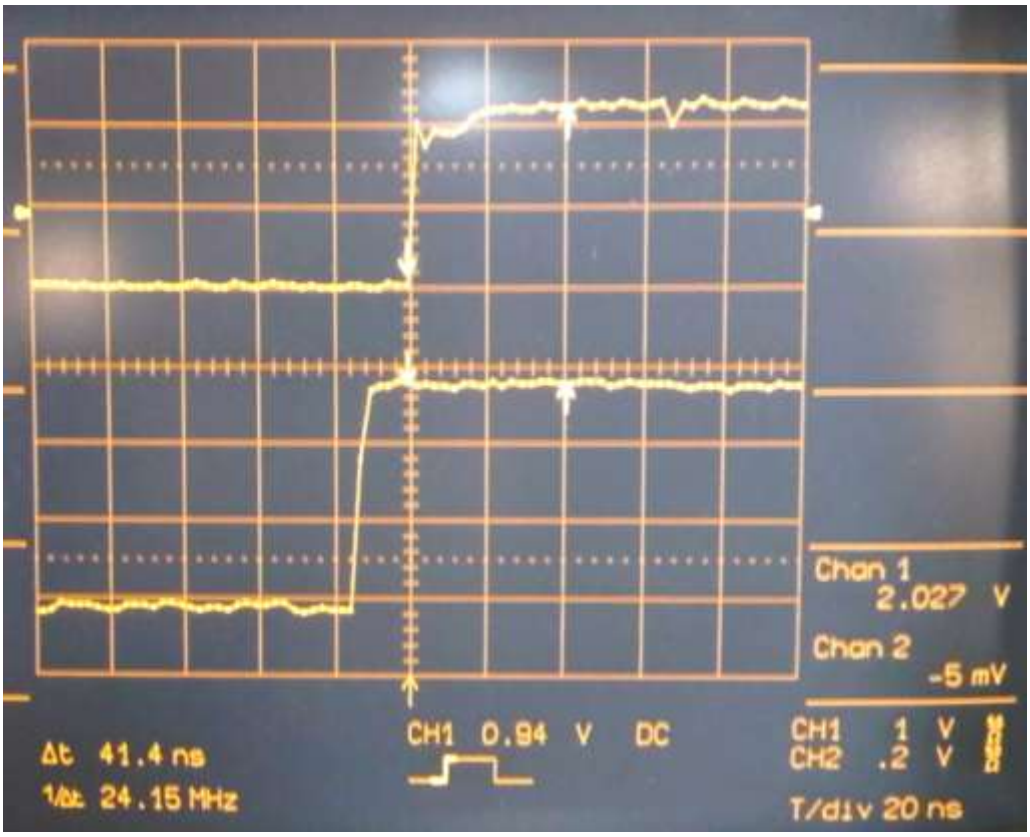
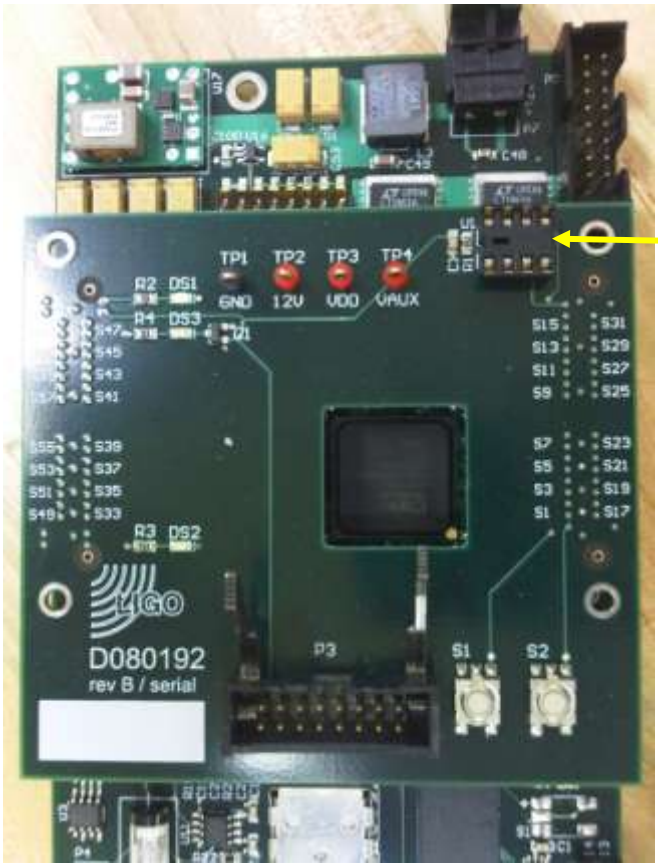


Figure 6 Test Daughterboard attached to the Slave board



APPENDIX. Programming FPGA Firmware onto Timing Module

The following step by step instruction describes the programming of the FPGA chip and Flash PROM on a Timing Module, such as the Master, FanOut or Slave modules. The guideline assumes that one has the following done/ready prior to going through the steps:
- Computer with Altium Designer is installed on it.
- Xilinx ISE WebPACK installed on the same computer.
- Altium USB-JTAG adapter.

1. Open Altium Designer.
2. Open 'My Account' from the 'DXP' menu bar (see Figure 1).
3. Press 'Sign In', provide your user name and password, then press 'Sign In' (see Figure 1).
4. Activate the product by clicking on the 'Activate' button (see Figure 1).

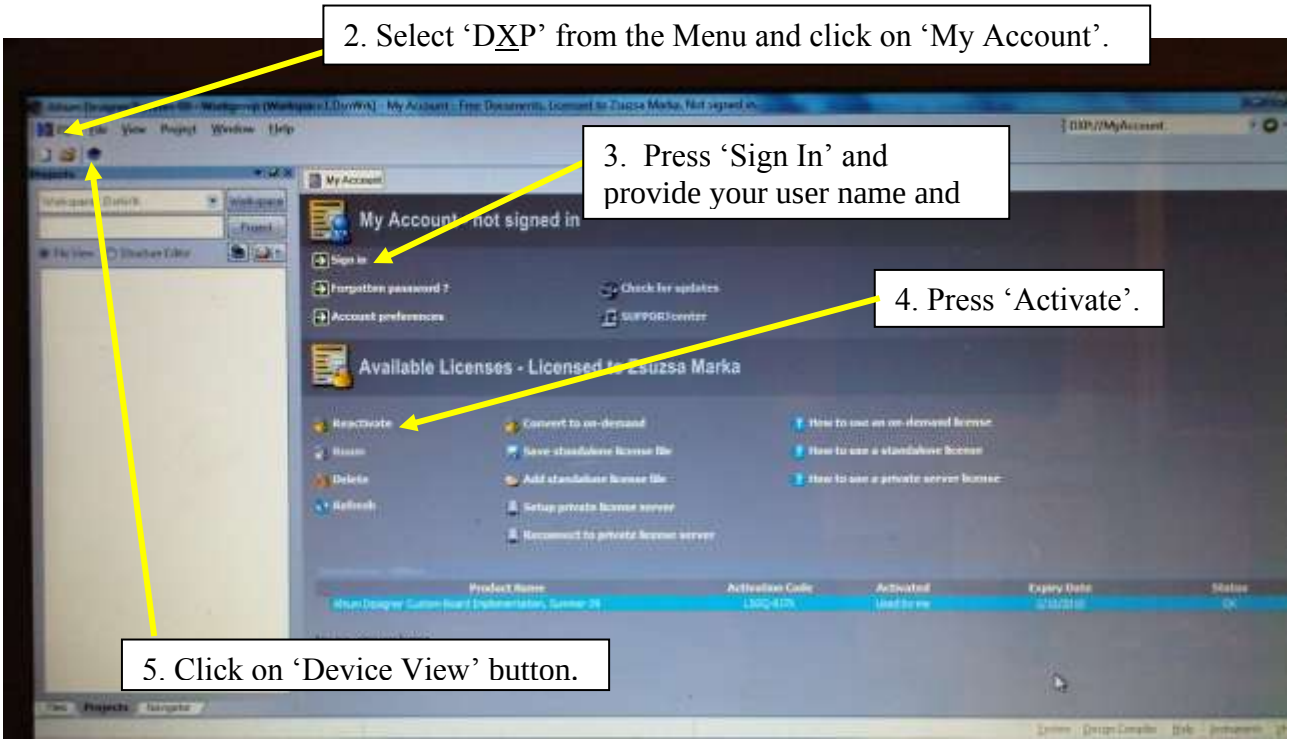


Figure 1. My Account window. The steps of signing in and activating an account that allows the use of the software are indicated. We also indicated the position of the Device View icon that opens the window from where FPGA programming will be done.

5. Click on 'Device View' button (see Figure 1).
6. Connect the computer to the desired board (Slave, Master or FanOut) using Altium USB-JTAG adapter.
7. Make sure that 'Live' is checked on the upper right corner of the 'Devices' screen in Altium Designer (see **Error! Reference source not found.**).

8. Make sure that 'Connected' is shown on the upper left corner of the screen (see **Error! Reference source not found.**).
9. Load Project. In the 'File' menu bar of Altium Designer, click on 'Open Project'. Select the the project you want to open and open it. Here, we give project locations for project one needs for testing:

   SLAVE TEST: C:\Timing\Slave_Test\FPGASlave.PrjFpg
   DUOTONE TEST: C:\Timing\DuoTone_Test\FPGADuoTone_TEST.PrjFpg

10. Reset Flash PROM. Right-click on Flash PROM icon as shown in **Error! Reference source not found.**. Click on 'Reset Hard Device'. Note that resetting can take up to a few minutes. Progress is indicated on the lower left corner of the screen.
11. Upload FPGA program to Flash PROM. Right-click on Flash PROM icon as in the previous step, and click on 'Choose File and Download…' (see **Error! Reference source not found.**).
    The files you need to select and download for testing are given below:

    SLAVE TEST:
    C:\Timing\Slave_Test\ProjectOutputs\Spartan3\fpgaslave.mcs
    DUOTONE TEST:
    C:\Timing\DuoTone_Test\ProjectOutputs\Spartan3\fpgaduotone_test.mcs

    Note that uploading the code can take up to a few minutes. Progress is indicated on the lower left corner of the screen.
12. Select project to program. From the menu below the FPGA chip icon, as indicated in **Error! Reference source not found.**, select the project you want to program. The project names for testing are:

    SLAVE TEST: FPGASlave / Spartan3
    DUOTONE TEST: FPGADuoTone_TEST / Spartan3

13. Program FPGA chip. Above the FPGA chip icon, click on 'Program FPGA', as indicated in **Error! Reference source not found.**.
14. For some tests you will need to use JTAG soft devices. These will appear after programming the board on the lower part of the 'Devices' screen, as indicated in **Error! Reference source not found.**. Note that soft devices work only if the board is connected to the computer with the Altium USB-JTAG adapter, it is programmed and the right project is selected below the FPGA icon that the board was programmed with.