LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
CALIFORNIA INSTITUTE OF TECHNOLOGY
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Testing procedure for the Timing Master/FanOut Chassis for Advanced LIGO

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This is an internal working note
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Front board document LIGO DCC # D**070011 - revision B**

Rear board document LIGO DCC# **D080094 - revision D**

Board Serial # (Front/Rear) _____

Board Type

Master ☐
- ☐ **on-board GPS receiver**
- ☐ **OCXO included**

FanOut ☐

Test Engineer (parts 1-5,7,9-10):

Test Date:

Test Engineer (parts 6,8):

Test Date:

Overall MFO chassis testing: ☐ PASSED ☐ FAILED

Signature/Initials:

Testing schedule:

1. Power Supply Unit (PSU) & on-board voltages
2. Flash PROM & JTAG Interfaces
3. Fiber I/O channels
4. The VCXO circuitry
5. Front-panel LEDs
6. GPS receiver, antenna & interface*
7. Fiber-delay claculator
8. OCXO interface & PLL circuitry**
9. BNC ports
10. Serial Interface (RS422)

Physical requirements:

Hardware:

1	GPS-antenna*
2	Altium USB JTAG Adapter. (refer to figure 2 in appendix)
3	12V, 2A PSU and 24V, 0.25A PSU and 2 cords with 3-pin D-sub connectors
4	Voltmeter
5	17 fiber-optic multi-mode (e.g. Agilent® HFBR 57E0/OR 57EOPZ) and at least 1 single-mode (e.g. Avago® AFCT-5760) transceiver modules
6	Windows®-operated PC with serial and parallel ports
7	RS232 to RS422 converter (BlackBox converter) See appendix for setup pictures.
8	Reference clocking (i.e. 1PPS) source w. optical output. E.g. a working MFO chassis LIGO D070011/D08094
9	An LC-LC fiber pair and a long (≥ 20m) optical fiber loop
10	BNC patch cable

Software:

1	MS Windows® 2000, XP
2	Altium® Designer v Summer 09
3	Motorola® WinOncore v1.2*
4	HHD Software Free Serial Port Monitor v3.31 http://www.serial-port-monitor.com/index.html
5	GPS clock from LIGOTools*

A brief introduction to the Master/FanOut board functionality is given in the Appendix.
More detailed description of the proposed timing system can be found online at
http://www.ligo.caltech.edu/docs/T/T070218-00/

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*Master-board with GPS-module only

**Master-board with OCXO module only

1. Testing the on-board PSU voltages at various testpoints (master and fanout procedure)

External Power Supply Unit:
manufacturer:

model:

Digital Multimeter:
manufacturer:

model:

(1) Measure the applied external voltages and write them below:

Nominal: 12.0V ± 1.0V
Measured by Power Supply*:

At the board (TP10):

*no electrical connections to the MFO

(2) Measure the voltages at the testpoints and the current through the board and write them below:

TP5	*nominal*	3.0V ± 0.15V	*measured:*
TP7	*nominal:*	1.2V ± 0.06V	*measured:*
TP8	*nominal:*	10.0V ± 0.5V	*measured:*
TP9	*nominal:*	5.0V ± 0.25V	*measured:*
TP10	*nominal:*	12.0V ± 1.2V	*measured:*
TP11	*nominal:*	2.5V ± 0.12V	*measured:*
TP12	*nominal:*	1.8V ± 0.09V	*measured:*
TP18	*nominal:*	-10.0V ± 0.5V	*measured:*
TP19	*nominal:*	3.3V ± 0.16V	*measured:*
The current:	*nominal:*	0.5A ± 10%	*measured:*

(3) Now, insert pluggable transceivers into all 17 available slots simultaneously, measure the voltages and the current again and write them down below:

TP5	*nominal*	3.0V ± 0.15V	*measured:*
TP7	*nominal:*	1.2V ± 0.06V	*measured:*
TP6	*nominal:*	5.0V ± 0.25V	*measured:*
TP9	*nominal:*	5.0V ± 0.25V	*measured:*
TP10	*nominal:*	12.0V ± 1.2V	*measured:*
TP11	*nominal:*	2.5V ± 0.12V	*measured:*
TP12	*nominal:*	1.8V ± 0.09V	*measured:*
TP18	*nominal:*	-10.0V ± 0.5V	*measured:*
TP19	*nominal:*	3.3V ± 0.16V	*measured:*
The current:	*nominal:*	Below 1.9A	*measured:*

All the measurements are within the nominal ranges: ☐ YES ☐ NO

2. Testing Flash PROM & JTAG interfaces (master and fanout procedure)

Use Altium® Designer;
bit-files: **fpgamasterfanout_cclk.bit** (for "Spartan3E XC3S1600E-4FG320C"), **fpgamasterfanout.mcs** (for "XCF XCF08PFSG48C")[both in /project outputs/Spartan3 folder

The procedure:

(a) Turn OFF the power to the MFO, wait a few seconds;
(b) Turn the power ON;
(c) Open Altium® Designer, go to Devices View
If testing a previously tested board, reset both the Spartan chip and the Flash PROM. You can do this by right clicking them and clicking reset.
File – Open - Open Project… - *navigate to MasterFanout_Test directory [DESKTOP-> MasterFanout_Test]* choose FPGAMasterFanout.PrjFpg. This is the project file.
Choose "FPGAMasterFanout / Spartan3" from dropbox under Spartan XC3S1600E-4FG320C
Download the indicated bit-file onto Spartan3E XC3S1600E-4FG320C;
Click "Program FPGA" button above the Spartan chip.
Open the OSCILLATOR_FREQUENCIES FRQCNT2 soft instrument. Look for JTAG icon on upper left corner. It should say "0/0" or "1/0". (Record the programming status of the FPGA below).
(d) Open the "Spartan3E XC3S1600E-4FG320C" instrument [right click Spartan chip, click "instrument" which open the Instrument Rack. (the FPGA core), click on JTAG viewer panel, check the "Live Update" (on the bottom of the window) box and watch the FPGA pin indicators (the purple and pink box should show the pins moving around); record the observations below.
(e) Right-click on the "XCF XCF08PFSG48C" instrument (the Flash PROM), in the panel for the PROM click select "Choose and Download" and choose the fpgamasterfanout.mcs file.
(f) Upon completion of the download, turn off the power to the board, wait for a few seconds, then restore the power
(g) The FPGA should be automatically reprogrammed from the Flash PROM [To verify this right click FPGA, click instrument and look for green status indicator for a successfully programmed device]
(h) Indicate the success/failure of the reprogramming

FPGA programming status [part c] (check one):	successful*	☐	failed	☐
FPGA pin indicators [part d] (check one):	all steady	☐	changing*	☐
Flash PROM reprogramming [part g] (check one):	successful*	☐	failed	☐

*indicates normal JTAG and/or PROM operation

3. Test fiber I/O channels (master and fanout procedure)

Use Altium® Designer;

download bit-file: fpga_mfo_test_cclk.bit

The procedure:

(a) In Altium® Designer; open FO_IO_ROUTER instrument; set the TEST_INPUT to '1' and the INT_FGEN and the THRU_FIBER to '1' Be sure to click the arrows button on the right of the value to register the input;

(b) Open the BNC_FIBER_FREQUENCIES instrument click Counter Options, set the Counter Time Base to 67.108 MHz; click Mode button under COUNTER CHANNEL B until it is set to frequency mode.

(c) Observe and record the frequency displayed in the COUNTER CHANNEL B with and without reference clock source connected to the front-panel INPUT port (e.g. connect a fiber cable/optical tranceiver from an output of a master to the INPUT port of the board you are testing); write the results in the table below;

(d) Set INT_FGEN to '0' , THRU_FIBER to '1' and TEST_INPUT to '0'. Connect the reference clock source to the INPUT port (e.g. take the output from an output of a Master board via optical transceiver and fiber cable and connect to the INPUT of the board you are testing).
Make a fiber-optic loop to the port #1.
To make a fiber optic loop:
A fiber optic cable has two ends, A and B, both of which have a 1 and 2. To make a fiber optic loop connect 1A and 1B into a port.

(e) Confirm that the front-panel FanOut LEDs follow the values of CHOOSE_OUT[3..0] and CHOOSE_IN[3..0] (from the FO_IO_ROUTER instrument). On Altium the numbers are one less than the number on the board. So for example when CHOOSE_OUT[3..0] and CHOOSE_IN[3..0] are both set to '3' it means it is reading the input and output of port 4 ;

(f) Set both, CHOOSE_OUT[3..0] and CHOOSE_IN[3..0] to 0 (thus port 1);

(g) In the table below, record the frequency observed in the COUNTER_CHANNEL_B of the BNC_FIBER_FREQUENCIES instrument; Note: "Frequency While Disconnected" means when there is no fiber connected to the INPUT port of the board you are testing.

(h) Check PASS if the nominal and observed frequencies match or FAIL if they don't;

(i) Move the fiber-loop to the next port (FO #2);

(j) Increase the values of CHOOSE_OUT and CHOOSE_IN by 1;

(k) Repeat the recording;

(l) In the same fashion, proceed with the rest of the ports;

(m) Write the results in the provided table. Note** in the table for frequency while disconnected, as long as it shows some floating frequency other than the 8.389 Mhz, that is OK.

Port #	Frequency while disconnected		Frequency while connected		PASS (match)	FAIL (mismatch)
	nominal	observed	nominal	observed		
INPUT	not 8.389 MHz		8.389 MHz		☐	☐
FO #1	not 8.389 MHz		8.389 MHz		☐	☐
FO #2	not 8.389 MHz		8.389 MHz		☐	☐
FO #3	not 8.389 MHz		8.389 MHz		☐	☐
FO #4	not 8.389 MHz		8.389 MHz		☐	☐
FO #5	not 8.389 MHz		8.389 MHz		☐	☐
FO #6	not 8.389 MHz		8.389 MHz		☐	☐
FO #7	not 8.389 MHz		8.389 MHz		☐	☐
FO #8	not 8.389 MHz		8.389 MHz		☐	☐
FO #9	not 8.389 MHz		8.389 MHz		☐	☐
FO #10	not 8.389 MHz		8.389 MHz		☐	☐
FO #11	not 8.389 MHz		8.389 MHz		☐	☐
FO #12	not 8.389 MHz		8.389 MHz		☐	☐
FO #13	not 8.389 MHz		8.389 MHz		☐	☐
FO #14	not 8.389 MHz		8.389 MHz		☐	☐
FO #15	not 8.389 MHz		8.389 MHz		☐	☐
FO #16	not 8.389 MHz		8.389 MHz		☐	☐

All nominals were met: ☐ YES ☐ NO

4. Testing the VCXO circuitry (master and fanout procedure)

The following testing is done by measuring voltages at the VCXO-related testing points on the MFO board. The hardware-implemented VCXO phase-locking loop automatically synchronizes the on-board VCXO to the 8MHz signal from the front-panel INPUT port. The voltages at the testpoints indicate whether or not the proper synchronization takes place. ***Prior to taking the measurements, a master timing source MUST be connected to the front-panel INPUT channel.*** **The test points are located on the front board, on the "middle left." BE SURE TO UNPLUG THE OCXO FOR THIS PART (IF THE BOARD YOU ARE TESTING IS A MASTER BOARD). See Page 23 Appendix for pictures depicting this disconnection.**

VCXO voltages:

	Without synchronization **		With synchronization **	
	nominal	measured	nominal	measured
TP1 (ERR)	**~10V**		**5.0 ± 0.5V**	
TP2 (CTRL)	**~0V**		**2V...8V**	

**With synchronization means connecting a Master board's output (any of #1-16) to the INPUT port of the board you are testing. Without synchronization means to unplug this connection from the INPUT port of the board you are testing.

The voltages are within the nominal ranges: ☐ YES ☐ NO

*****Reconnect OCXO when done.***

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5. Test front-panel LEDs (master and fanout procedure)

This test checks the operational status of the front-panel LEDs.
Use Altium® Designer;
download bit-file: **fpgamasterfanout_cclk.bit**

The procedure:

(a) Open Altium® Designer, check if the FPGA is programmed with the correct bit-file to the FPGA. If not, download the correct bit file indicated above.
(b) Open the SERIAL_LED_ROUTER instrument
(c) Set TEST_LEDS flag to 1
(d) Increase the LED_RATE value from 00 to 3#, considering *only* the highest digit (# can be any number).
(e) Record the blinking rates in the provided table

Parameter	LED rate at 0#		LED rate at 3#	
	nominal	**observed**	**nominal**	**observed**
ON	steady		2/sec.	
1PPS	steady		2/sec.	
GPS	steady		2/sec.	
OCXO	steady		2/sec.	
INPUT	steady		2/sec.	
#1	steady		2/sec.	
#2	steady		2/sec.	
#3	steady		2/sec.	
#4	steady		2/sec.	
#5	steady		2/sec.	
#6	steady		2/sec.	
#7	steady		2/sec.	
#8	steady		2/sec.	
#9	steady		2/sec.	
#10	steady		2/sec.	
#11	steady		2/sec.	
#12	steady		2/sec.	
#13	steady		2/sec.	
#14	steady		2/sec.	
#15	steady		2/sec.	
#16	Steady		2/sec.	

All LEDs blink simultaneously: ☐ YES ☐ NO

***Set TEST_LEDS back to 0 when finished.

6. GPS antenna & receiver module test (MASTER only)

This test procedure can only be done at sites with GPS antenna access.

Use Altium® Designer, Motorola® WinOncore, GPSclock from LIGOtools;
download bit-file**: fpgamasterfanout_cclk.bit**

The procedure:
open Altium® Designer, download the bit-file

1.

Open Altium® Designer, check if the FPGA is programmed with the correct bit-file to the FPGA. If not, download the correct bit file indicated above.

Set up the instrument (OSCILLATOR_FREQUENCIES) in Altium® Designer:

(a) make sure each channel window is in the "Frequency" mode; to change the mode, press the Mode button below each screen as many times as necessary, until the windows gets into the desired mode.
(b) press the "Counter Options" button under the left screen; set up the Counter Time Base to 67.108 MHz.
(c) make sure the Run button is pressed, in which case it should have yellow color.

2. Connect the GPS antenna to the GPS port at the back panel of the MASTER chassis.

(a) Open the GPS_IO instrument.
(b) set the INITIALIZE output to '0'
(c) set the RS422_SEL output to '1'
(d) set the LOOPBACK output to '0'
(e) make sure the CLKD[31..0] output is set to 0x800000 or 8,388,608 decimal.
(f) wait a few seconds for the GPS_1PPS and PPS_INDICATIOR input indicators to begin toggling
(g) wait for additional 15 minutes for the GPS receiver to acquire data
(h) open WinOncore and perform GPS self-test; fill-up the table below
(i) in Altium® Designer, open the GPS_IO instrument again and record the status in the provided table

GPS self-test results:

Parameter	Nominal value	Factual value
Antenna Status	OK	
RTC comm. & time	PASS	
Temperature Sensor	PASS	
RAM	PASS	
ROM	PASS	
1 kHz Presence	PASS	
Temp. Sensor Data Checksum	PASS	
Oscillator Data Checksum	PASS	
Manufacturing Data Checksum	PASS	
Channel 12 correlation test	PASS	
Channel 11 correlation test	PASS	
Channel 10 correlation test	PASS	
Channel 9 correlation test	PASS	
Channel 8 correlation test	PASS	
Channel 7 correlation test	PASS	
Channel 6 correlation test	PASS	
Channel 5 correlation test	PASS	
Channel 4 correlation test	PASS	
Channel 3 correlation test	PASS	
Channel 2 correlation test	PASS	
Channel 1 correlation test	PASS	

GPS_IO instrument status:

Parameter	Nominal value	Factual value
# of tracked GPS satellites	≥ 3	
# of visible GPS satellites	≥ (# of tracked)	
LOCKED value	TRUE	
Highest 3 bits of GPS_STATUS	111	
ERROR value	FALSE	
Value of GPS_SECOND	Use reference*	
GPS_SECOND discrepancy with the reference*	0	

All the nominal values have been met: ☐ YES ☐ NO

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7. Test fiber-delay calculator (master and fanout procedure)

Use Altium® Designer;
download bit-file: **fpgamasterfanout_cclk.bit**

Altium® virtual instrument I/O reference:

The instrument (DELAY_MEASURE) setup:

(a) Open Altium® Designer, check if the FPGA is programmed with the correct bit-file to the FPGA. If not, download the correct bit file indicated above.

(b) Open the DELAY_MEASURE soft instrument in Altium Designer. Connect the longest possible fiber loop (up to $\mathbf{10^8}$ m) to the FanOut-port #**1. Be sure the cable is at least several tens of meters, (i.e. do not use only 3m). SEE APPENDIX C FOR PICTURES SHOWING HOW TO MAKE THE FIBRE LOOP FOR THIS PART**

(c) For the given fiber length, calculate* the nominals and write them in the spaces provided below

(d) Observe and record the actual measured delays

*For every **1000m** of the fiber, the measured delay shown in DEL_CNT[31..0] and ALT_CNT[31..0] should be about **335** units (i.e. clock-cycles). E.g. the measured delay for the 4km+ loop at LIGO-Hanford was 1489 at both counters.

For the fiber-loop of length

CLK_CNT[31..0]:	nominal:	67,108,854	measured:
DEL_CNT[31..0]:	nominal:		measured:
ALT_CNT[31..0]:	nominal:		measured:

Notes:

8. Testing the OCXO interface (MASTER only) NOT REQUIRED AT MANUFACTURING SITE

Use Altium® Designer, HHD Software Free Serial Port Monitor;
download bit-file: **fpgamasterfanout_cclk.bit**

Altium® virtual instrument I/O reference:

The procedure:

(a) Open Altium® Designer, check if the FPGA is programmed with the correct bit-file to the FPGA. If not, download the correct bit file indicated above.
(b) Open the OCXO_MONITOR instrument
(c) Unscrew the OCXO manual adjustment cap on the OCXO chassis
(d) Using small flat screwdriver, adjust the OCXO so that the value in the OCXO_DEV[15..0] is no greater than 3. ***Be very gentle,*** *as the OCXO's internal adjustment knob is very easy to break. Use counter-clockwise motion for the OCXO_DEV to go towards the positive side.*
(e) Open the FILTER_INPUT_SWITCH instrument
(f) Set INP_SEL flag to HIGH (green); make sure the RESET_FILTER flag is LOW(red)

(g) Open Free Serial Port Monitor, go to Console Window
(h) Open a new connection (COM1, 9600-baud, 8-bits, no-parity)
(i) Allow ~20min for the filter to settle down, then go to the Port Monitor's Console Window and record the string value below

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OCXO status serial data format:

The OCXO status string has the following structure:

[flags][hex_error][hex_correction][dec_error][dec_correction][hex_fiber_delay] …

where the fields are separated by spaces.

Char. 1	OCXO LOCKED flag
Char. 2	FILTER OVERFLOW flag
Char. 3	field separator (space)
Char. 4	OCXO error sign
Char. 5..12	OCXO error value in hex base (8-digit number)
Char. 13	field separator (space)
Char. 14	OCXO control sign
Char. 15..18	OCXO control value in hex base (4-digit number)
Char. 19	field separator (space)
Char. 20	OCXO error sign
Char. 21..28	OCXO error value in decimal base (8-digit number)
Char. 29	field separator (space)
Char. 30	OCXO control sign
Char. 31..35	OCXO control value in decimal base (5-digit number)
Char. 36	field separator (space)
Char. 37..44	fiber-delay (clock-cycles in hex base; not used for OCXO testing)

Allowing ~20min. for the OCXO synchronization, fill in the table below:

OCXO LOCKED flag (Char 1)	nominal: 1	observed:
FILTER OVERFLOW flag (Char2)	nominal: 0	observed:
OCXO error (decimal) (Char 21..28)	nominal: 0 ± 4	observed:

9. Testing BNC ports (master and fanout procedure)

Use Altium® Designer;
download bit-file: **fpgamasterfanout_cclk.bit**

The procedure:

(a) Connect the 1PPS_OUT and 1PPS_IN ports to eachother via coaxial cable on back panel of MFO chassis.;
(b) Open Altium® Designer, check if the FPGA is programmed with the correct bit-file to the FPGA. If not, download the correct bit file indicated above.
(c) Open the BNC_FIBER_FREQUENCIES instrument;
(d) In the "Counter Options" set the Counter Time Base to 67.108 MHz;
(e) Open the FO_IO_ROUTER instrument;
(f) Disable the THRU_FIBER (the indicator turns *red*);
(g) Record the listed values below

Value in COUNTER_CHANNEL_A:	Nominal:	8.389 MHz
	Displayed:	
MONITOR indicator toggling rate:	Nominal:	1 per second
	Observed:	

Notes:

10. Testing the serial interface – RS422 output (master and fanout procedure)

This test verifies the operational status of the on-board serial interfaces.

Use Altium® Designer, Microsoft HyperTerminal;
download bit-file: **fpgamfo_cclk.bit, fpgamfo.mcs**

The procedure:

(a) Turn OFF the power to the MFO via back of board (unplug 12V,24V), wait a few seconds;
(b) Turn the power ON;
(c) In Altium® Designer, go to Devices View
If testing a previously tested board, reset both the Spartan chip and the Flash PROM. You can do this by right clicking them and clicking reset.
File – Open - Open Project… - *navigate to* ***MasterFanout*** *(*****NOT THE TEST)*** *directory* (see appendix for file locations)
choose FPGAMFO.PrjFpg. This is the project file.
Choose FPGAMFO/ Spartan3 from dropbox under Spartan XC3S1600E-4FG320C
Download fpgamfo_cclk.bit onto Spartan3E XC3S1600E-4FG320C; Click Program FGPA above the Spartan chip.

(d) Right-click on the "XCF XCF08PFSG48C" instrument (the Flash PROM), in the panel for the PROM click select "Choose and Download" and choose the FPGAMFO.mcs file.
(e) Upon completion of the download, turn off the power to the board, wait for a few seconds, then restore the power
(f) The FPGA should be automatically reprogrammed from the Flash PROM [To verify this right click FPGA, click instrument and look for green status indicator for a successfully programmed device]
(g) Set up Lantronix/RS422 connection. Thus plug one end into RS422 port on back of board. Then plug other end into Lantronix box Serial port 1. Hook up Ethernet cable, and power cable into Lantronix box.
(h) Open Microsoft HyperTerminal in windows.
(i) Click new connection. Name it anything (example: RS422)
(j) Set up by connecting with a TCP/IP connection. Enter the IP address (192.168.1.25) of the Lantronix box as the Host Address. Enter the port number of the lantronix box (10001).
(k) You should see repeating sections of text appear in the command window containing the words "LIGO TIMING SYSTEM" along with other arbitrary symbols. Note the success/failure of this below.

"LIGO" commands in HyperTerminal: ☐ present ☐ absent

RS422 operates properly: ☐ YES ☐ NO

Testing summary

For each test, indicate the results in the table below:

On-board voltages	☐ PASS	☐ FAIL	
VCXO circuitry	☐ PASS	☐ FAIL	
PROM & JTAG interfaces	☐ PASS	☐ FAIL	
Front-panel LED circuits	☐ PASS	☐ FAIL	
GPS antenna & receiver	☐ PASS	☐ FAIL	☐ N/A
Fiber I/O channels	☐ PASS	☐ FAIL	
Fiber-delay calculator	☐ PASS	☐ FAIL	
OCXO interface	☐ PASS	☐ FAIL	☐ N/A
BNC ports	☐ PASS	☐ FAIL	
Serial interfaces	☐ PASS	☐ FAIL	

Overall MFO board testing: ☐ PASSED ☐ FAILED

Test Engineer (parts 1-5,7,9-10):

Test Date for parts 1-5,7,9-10:

Test Engineer (parts 6,8):

Test Date:

Additional Comments:

Appendix A:

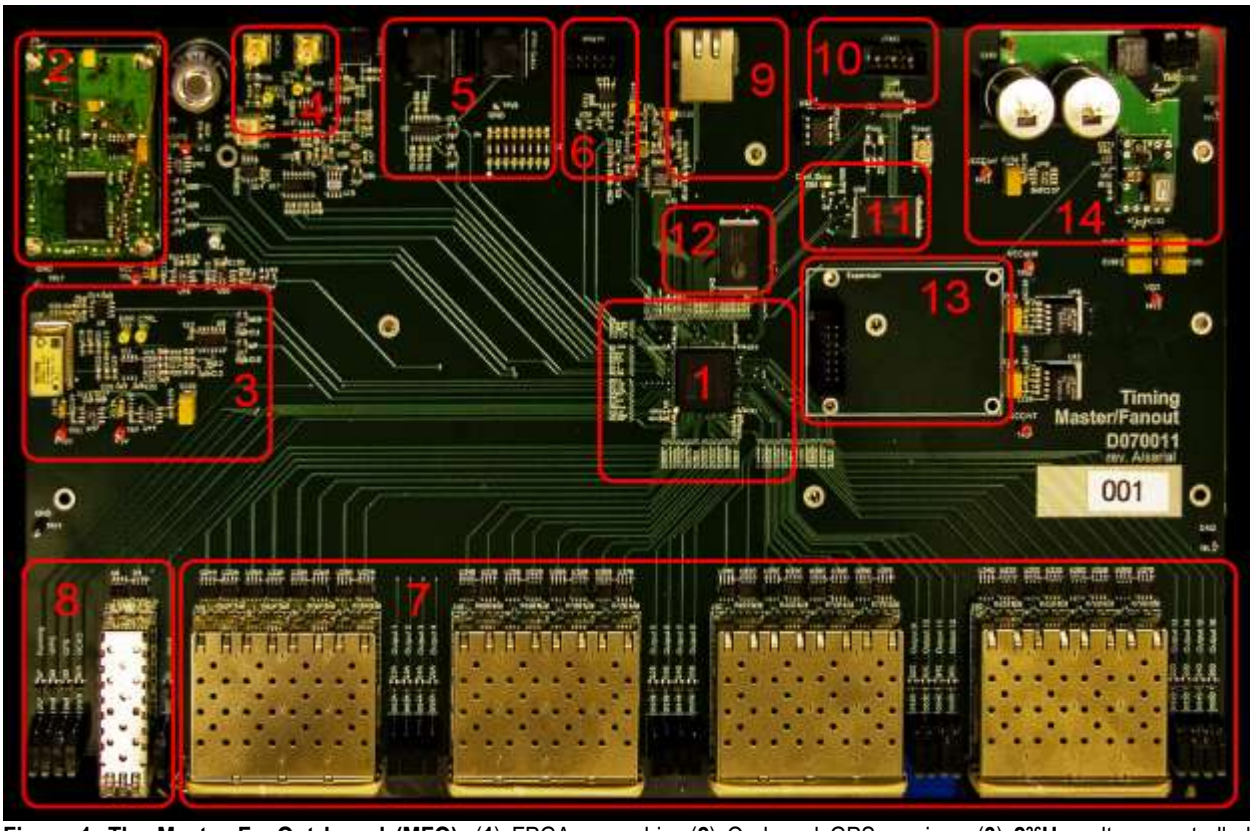


Figure 1. The Master FanOut board (MFO). (**1**) FPGA core chip. (**2**) On-board GPS-receiver. (**3**) **2^{26}Hz** voltage-controlled oscillator, used as internal clock. (**4**) The port for connecting external oven-stabilized **2^{26}Hz** oscillator. (**5**) BNC port for connecting to the external 1PPS source. (**6**) General purpose RS422 port. (**7**) 16 optical I/O FanOut channels. (**8**) Uplink optical I/O channel. (**9**) General purpose Ethernet port. (**10**) JTAG port for external programming of the FPGA. (**11**) Flash memory chip (used for programming FPGA). (**12**) RAM block. (**13**) Optional slot (currently used for mounting JTAG programming device). (**14**) The power supply unit.

The figure above shows the main blocks of the Master/FanOut board. The primary goal of the board is to acquire and distribute precise timing information with an accuracy of better than 1us, according to the requirements. To perform all the necessary calculations, we use a special logic element called Field-Programmable Gate Array, or FPGA (block #1 of the figure 1). The FPGA is in a sense a reduced version of a Central Processing Unit (CPU) alike those commonly found in computers. It uses the VCXO (block #3 on the figure) as its clocking device for the internal logic. While the VCXO is well suitable for driving the FPGA logic, its precision does not meet the 1us requirement. To overcome this, the VCXO is synchronized to a much more stable oven-controlled oscillator (OCXO) through the external port (block #4) which in its turn is synchronized to either the reference clocking signal received from the optical INPUT port (block #8), an alternative RF coaxial input (block #5) or the on-board GPS receiver (block #2). This given synchronization hierarchy is expected to hold the internal FPGA clock discrepancy within the 1us window.

The distinct feature of an FPGA is its ability to be programmed in a way similar to an ordinary CPU. The programming environment in our case is the PC-based Altium® Designer software package. The communication between the PC and the FPGA is done through the parallel port of the computer and the JTAG port of the Master/FanOut board (block #10). The programming code is stored in the flash-ROM module (block #11). All the communications with the PC, other than programming, are routed through either a serial port (block #6) or Ethernet interface (block #9, not tested here). The distribution of timing information to the devices other than PC goes through the 16 optical FanOut ports (block #7).

For more information, look the online documentation posted at
http://www.ligo.caltech.edu/docs/T/T070218-00/

Appendix B: Altium® virtual instrument I/O reference:

FO_IO_ROUTER - routes the signal through chosen optical I/O FanOut (FO);

BIN[15..0]	-	monitors the active/inactive status of the FanOuts;
MONITOR	-	toggles when 1PPS signal is received;
INT_FGEN	-	when enabled, switches to internal frequency generator(CLKGEN); When disabled, the output is SYNCIN
THRU_FIBER	-	when enabled, routes the 8MHz signal through the chosen FO; When disabled, the output is the back panel 1PPS
CHOOSE_OUT[3..0]	-	allows to choose FO output;
CHOOSE_IN[3..0]	-	allows to choose FO input;
TEST INPUT	-	when enabled the output is the front panel INPUT's input When disabled, the output is the FO input

DELAY_MEASURE - shows the time required for the signal to go through the loop of fiber connected to an optical I/O port;

CLK_CNT[31..0]	counts the number of clock-cycles in one second
DEL_CNT[31..0]	shows the propagation delay in units of clock-cycles
ALT_CNT[31..0]	same function as DEL_CNT[31..0] but alternative implementation; may be used for verification
NO_SIGNAL	displays the presence of the attached fiber-loop
LED_ON	when enabled, sends the toggling 1PPS signal to the LED of the FanOut-1, overriding other signals for this LED.

BNC_FIBER_FREQUENCIES - measures the frequency of the incoming signal through a given port;

COUNTER_CHANNEL_A	the signal frequency of the BNC "1PPS output" port;
COUNTER_CHANNEL_B	the signal frequency of the chosen FanOut port.

SERIAL_LED_ROUTER routes the signals between serial interfaces (on-board GPS receiver & RS422 port) as well as front-panel LEDs.

A[7..0]	not used
GPS_THRU	connects GPS and RS422 interfaces directly, bypassing all the FPGA logic
OCXO_GPS_TO_RS422	chooses between the OCXO and the GPS data to be sent through the RS422 port
TEST_LEDS	for LED testing purposes, overrides all other FPGA LED-driving circuitry and sets all the front-panel LEDs in test mode
LED_RATE[7..0]	sets the blinking rate for the front-panel LEDs

FILTER_INPUT_SWITCH - controls the input of the OCXO-regulating filter.

OUT_VAL[31..0]	displays the combined output value of the COARSE[10..0], FINE[11..0] and SFINE[11..0] controls
FOUT[31..0]	graphically shows the output value of the OCXO-regulating filter
FONUM[31..0]	numerical equivalent of FOUT[31..0]
OVF	indicates the overflow status of the filter

IOLD[31..0]	reflects the error value previously stored in the filter
TO_DAC[15..0]	shows the value sent to the OCXO-controlling DAC
SIGN	shows the sign of the DAC value
O_F	indicates the overflow status of the DAC value
COARSE[10..0]	simulates the filter error input with full range but minimal resolution
FINE[11..0]	same as COARSE[10..0] but with medium range and resolution
SFINE[11..0]	same as COARSE[10..0] but with minimal range and highest resolution
INP_SEL	toggles the filter input between simulation (disabled, red) and actual (enabled, green) inputs
SUPER_GAIN[3..0]	applied additional gain (i.e. bit-shift) to the filter output (currently disabled and non-functional)
SG_BYPASS	allows bypassing the applied super-gain (currently disabled and non-functional)
RESET_FILTER	resets the memory within the filter
SYNC_OVERRIDE	forces synchronization of the VCXO to the optical input

OCXO_MONITOR - monitors various OCXO parameters.

OCXO_PRESENT	detects the active presence of the OCXO
ONEPPS_EXT	reflects the presence of an external 1PPS signal
ONEPPS_INT	toggles along with the internal 1PPS generator
OCXO_LOCKED	goes high whenever the OCXO error is below the threshold
OCXO_ERR[31..0]	displays the OCXO error value
FM[31..0]	monitors the input value of the OCXO filter engine
OCXO_CTRL[15..0]	displays the OCXO-adjusting value sent to the DAC circuit, 0x8000 corresponding to zero-adjustment
OCXO_DEV[15..0]	reflects the absolute value of the OCXO deviation from the reference clock in terms of clock-cycles per-second
OCXO_DEV_SIGN	GREEN indicates the POSITIVE sign of the OCXO deviation

OSCILLATOR_FREQUENCIES - shows the frequencies of the onboard/external oscillators;

COUNTER CHANNEL A	-	GPS 1PPS signal frequency, nominally 1Hz
COUNTER CHANNEL B	-	The frequency of the external OCXO, in MHz.

DELAY_MEASURE - shows the time required for the signal to go through the loop of fiber connected to an optical I/O port;

CLK_CNT[31..0]	counts the number of clock-cycles in one second
DEL_CNT[31..0]	shows the propagation delay in units of clock-cycles
ALT_CNT[31..0]	same function as DEL_CNT[31..0] but alternative implementation; may be used for verification
NO_SIGNAL	displays the presence of the attached fiber-loop
LED_ON	when enabled, sends the toggling 1PPS signal to the LED of the FanOut-1, overriding other signals for this LED.

GPS_I0 - reads and displays various GPS-receiver data parameters;

Inputs:

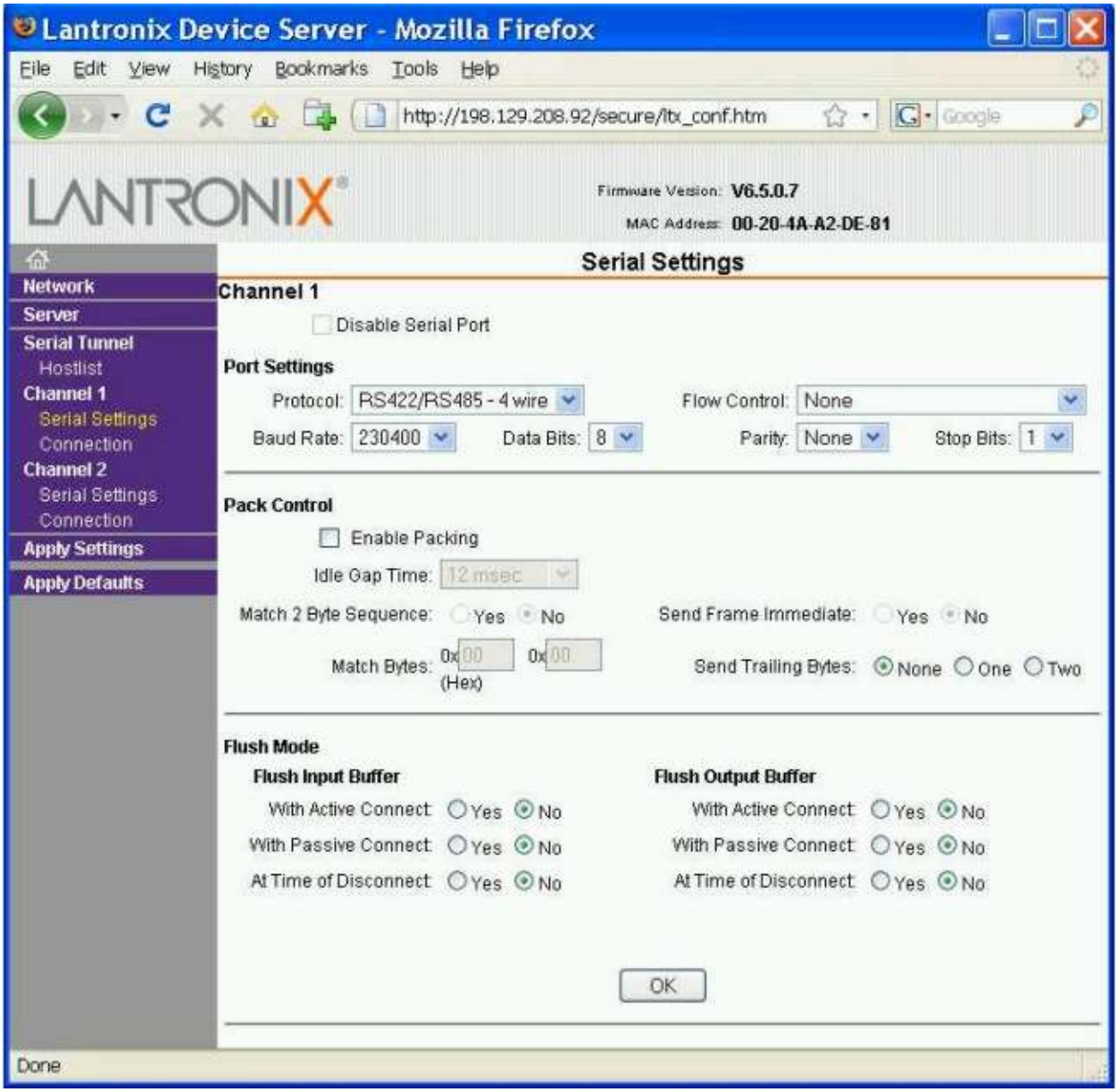
GPS_SECOND[31..0]	-	The 32-bit value of the current GPS-second
VISIBLE[7..0]	-	The number of visible satellites
TRACKED[7..0]	-	The number of tracked satellites
GPS_STATUS[15..0]	-	GPS receiver status
ID1_TAG[31..0]	-	GPS-receiver ID-tag, highest 16 bits
ID2_TAG[31..0]	-	GPS-receiver ID-tag, lowest 16 bits
LOCKED	-	Confirms locking to GPS satellites
GPS_1PPS	-	Changes state each time the 1PPS is received
PPS_INDICATOR[15..0]	-	Scopes the GPS_1PPS line with 1/8 sec. resolution
ERROR	-	The software error status.

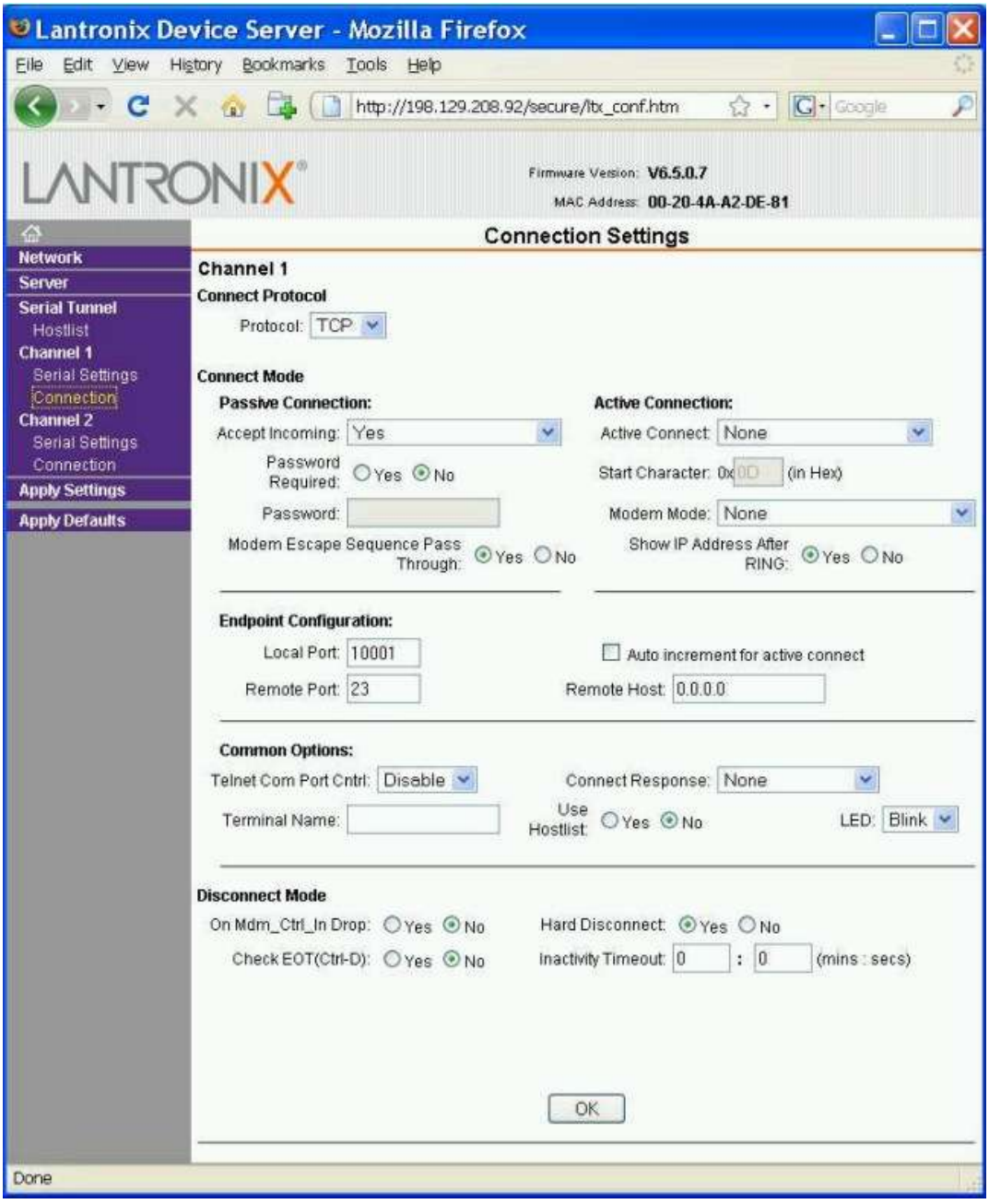
Outputs:

INITIALIZE	-	sends initialization signal
RS232_SEL	-	selects the source for the serial output
LOOPBACK	-	loops the output signal back to the software receiver
CLKD[31..0]	-	sets the clock division factor for the PPS_INDICATOR

APPENDIX C. Lantronix UDS2100 Configuration.

The picture below shows an example for Lantronix UDS2100 configuration. The UDS2100 module can be accessed and configured through the internet using its assigned IP address. Tthe IP address varies for every Lantronix module. One can obtain the IP address for a Lantronix module using the software given with it. See the Lantronix manual for further instructions.





Appendix D: Setup Pictures:

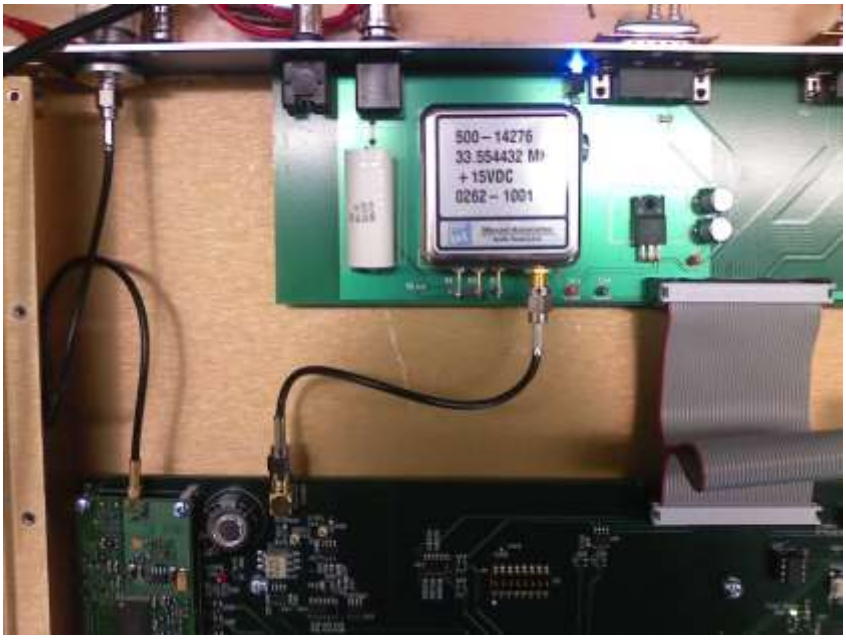
Figure 2 JTAG Interface

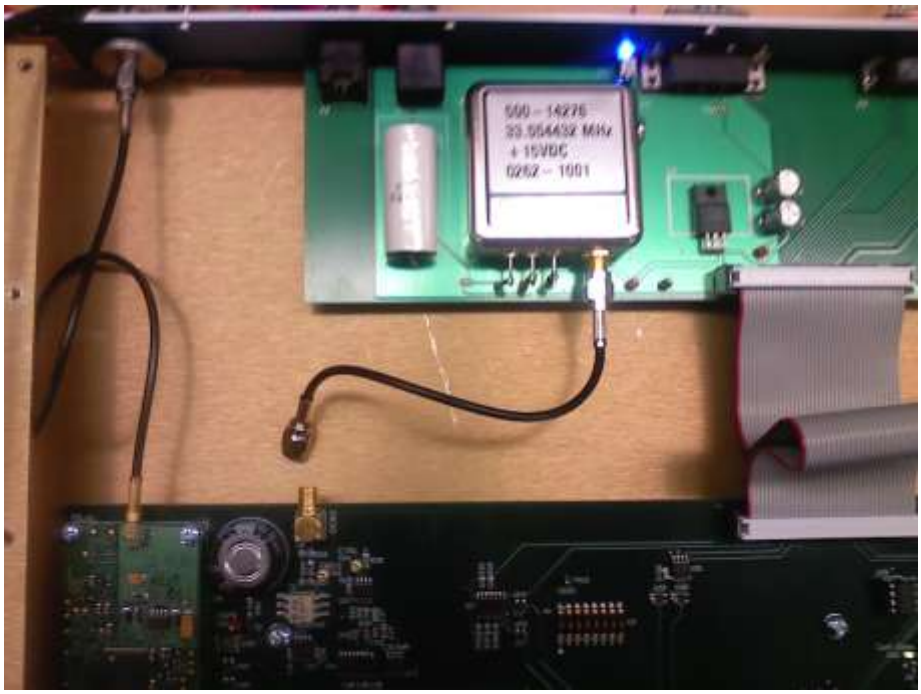
Note: The JTAG Interface needs to connect to a laptop/computer via a USB (for power) and the other end connects to the JTAG connector on

The master board

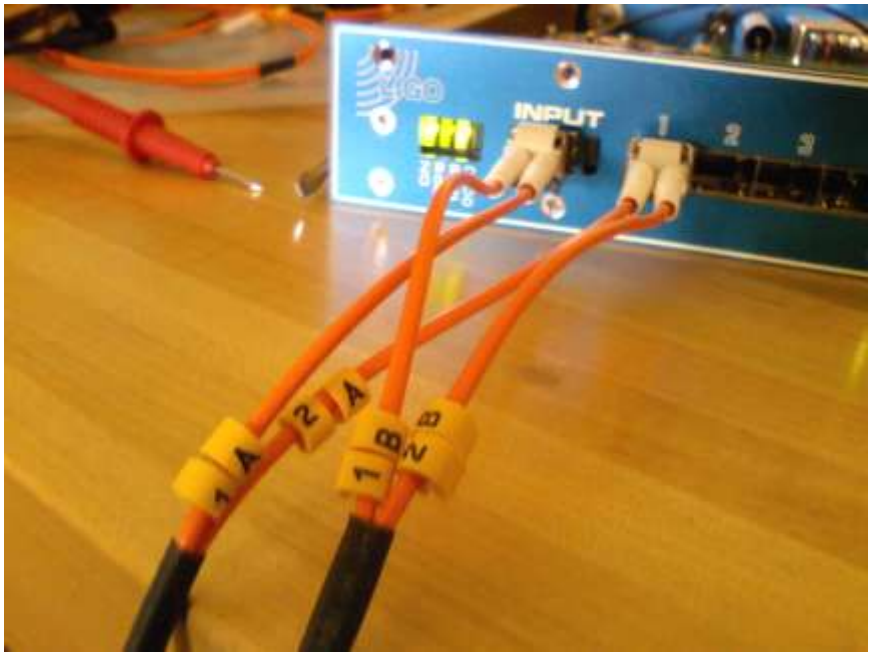
TESTING THE VCXO CIRCUITRY

For part 4, the OCXO must be disconnected and connected. Below are pictures depicting this. The OCXO is the Big silver box next to the big Capacitor on the rear board.

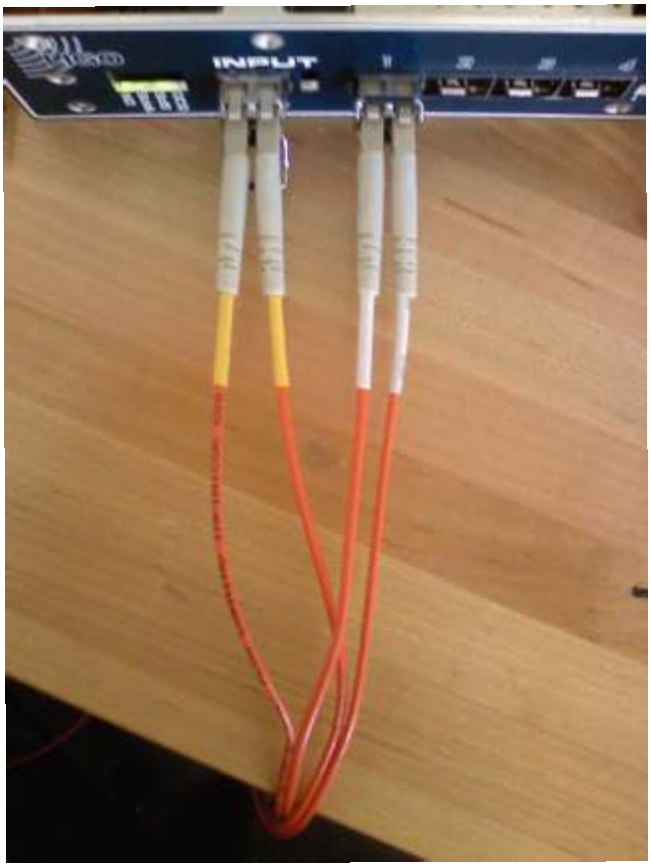




FIBRE DELAY LOOP (Part 7 – Test Fiber- Delay Calculator)



If wires are NOT labeled:



ALTIUM DESIGNER SETUP

The following step by step instruction describes the programming of the FPGA chip and Flash PROM on a Timing Module, such as the Master, FanOut or Slave modules. The guideline assumes that one has the following done/ready prior to going through the steps:
- Computer with Altium Designer is installed on it.
- Xilinx ISE WebPACK installed on the same computer.
- Altium USB-JTAG adapter.

1. Open Altium Designer.
2. Open 'My Account' from the 'DXP' menu bar (see Figure 1).
3. Press 'Sign In', provide your user name and password, then press 'Sign In' (see Figure 1).
4. Activate the product by clicking on the 'Activate' button (see Figure 1).

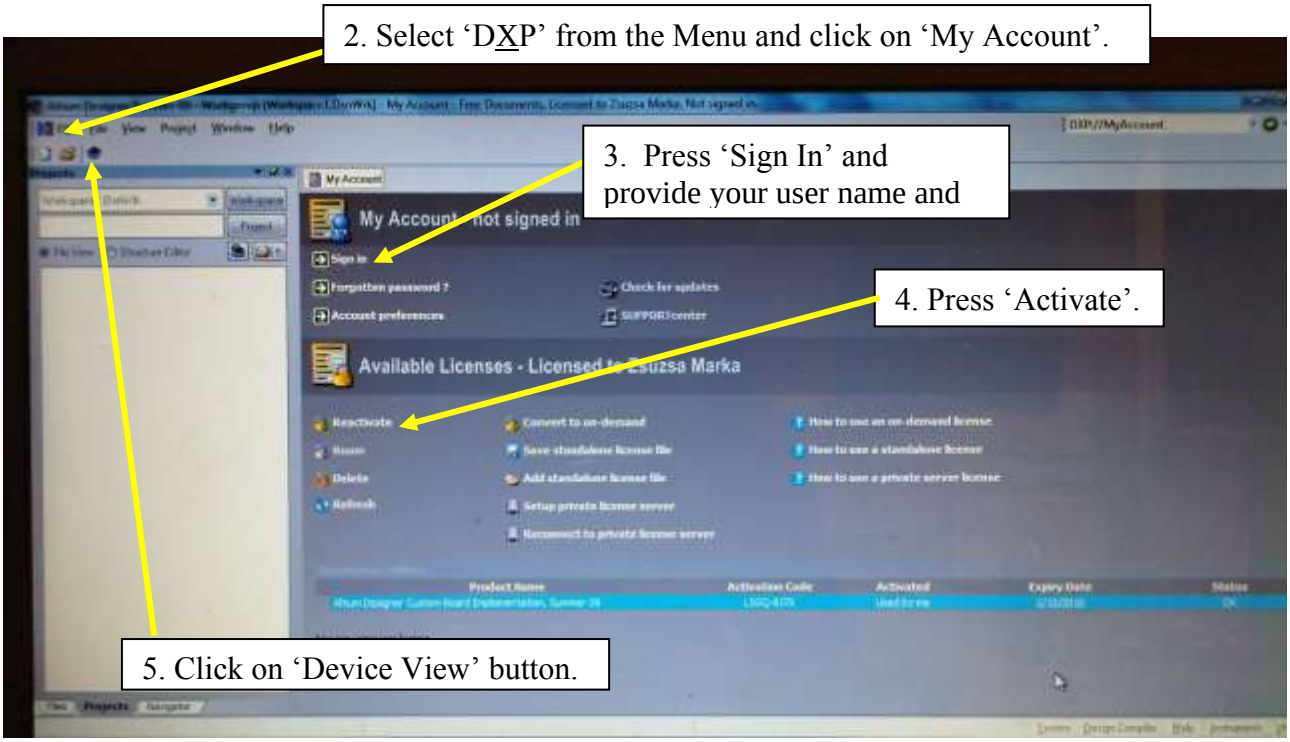


Figure 1. My Account window. The steps of signing in and activating an account that allows the use of the software are indicated. We also indicated the position of the Device View icon that opens the window from where FPGA programming will be done.

5. Click on 'Device View' button (see Figure 1).
6. Connect the computer to the desired board (Slave, Master or FanOut) using Altium USB-JTAG adapter.
7. Make sure that 'Live' is checked on the upper right corner of the 'Devices' screen in Altium Designer (see **Error! Reference source not found.**).
8. Make sure that 'Connected' is shown on the upper left corner of the screen (see **Error! Reference source not found.**).

9. Load Project. In the 'File' menu bar of Altium Designer, click on 'Open Project'. Select the the project you want to open and open it. Here, we give project locations for project one needs for testing:

   MASTER FANOUT TEST:
   C:\Documents and Settings \ Imre Bartos\Desktop\052710\FPGA-VHDL\MasterFanout_Test\FPGA_MFO_TEST.PRJFPG
   MASTER FANOUT:
   C:\Documents and Settings\Imre Bartos\Desktop\052710\FPGA-VHDL\MasterFanout\FPGAMFO.PRJFPG

10. Reset Flash PROM. Right-click on Flash PROM icon as shown in **Error! Reference source not found.**. Click on 'Reset Hard Device'. Note that resetting can take up to a few minutes. Progress is indicated on the lower left corner of the screen.
11. Upload FPGA program to Flash PROM. Right-click on Flash PROM icon as in the previous step, and click on 'Choose File and Download…' (see **Error! Reference source not found.**).
    The files you need to select and download for testing are given below:

    MASTER FANOUT TEST:
    C:\Documents and Settings \ Imre Bartos\Desktop\052710\FPGA-VHDL\MasterFanout_Test\ProjectOutputs\Spartan3\fpga_mfo_test.mcs

    Note that uploading the code can take up to a few minutes. Progress is indicated on the lower left corner of the screen.
12. Select project to program. From the menu below the FPGA chip icon, as indicated in **Error! Reference source not found.**, select the project you want to program. The project names for testing are:

    MASTER FANOUT TEST: FPGA_MFO_TEST / Spartan3

13. Program FPGA chip. Above the FPGA chip icon, click on 'Program FPGA', as indicated in **Error! Reference source not found.**.
14. For some tests you will need to use JTAG soft devices. These will appear after programming the board on the lower part of the 'Devices' screen, as indicated in **Error! Reference source not found.**. Note that soft devices work only if the board is connected to the computer with the Altium USB-JTAG adapter, it is programmed and the right project is selected below the FPGA icon that the board was programmed with.