LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

-LIGO-

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AdL Triple Low Current Driver Final Design Report		
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1 Introduction

The document describes the final design of the AdL Triple Suspension Low Current Coil Driver. The driver will be used as the driver electronics for the middle stage of the IMC and Cavity Triple Suspensions used in AdLIGO. The design was done collaboratively between the US and UK design teams. The prototype unit was built and tested at CIT. The production units will be fabricated by the UK.

The figure below shows the naming conventions and locations of the triple suspensions stages. The middle stage is shown in blue.

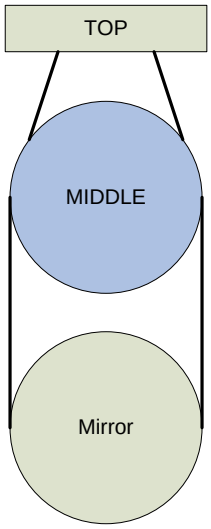

Figure 1: AdL Triple SUS Stages

2 Requirements

The requirements for all AdL Triple Suspension Electronics can be found in LIGO document T080065-E1-C, "AdL Beam Splitter, Input Mode Cleaner, Large Recycling and Small Recycling Triple Suspension Electronics Requirements". For the Low Current Coil Driver the "important" requirements are output current noise and dynamic range.

- Output Current Noise Requirement: 125 pA/√Hz, for 10Hz<freq<15Hz
- Dynamic Range: $3mA_{peak}$, for freq<1KHz.

Other requirements such as input voltages and monitoring points are called out in the requirements document.

3 Design

The schematic for the board can be found in LIGO document D0900884-v1. The figure below shows the design for a single channel of the driver board.

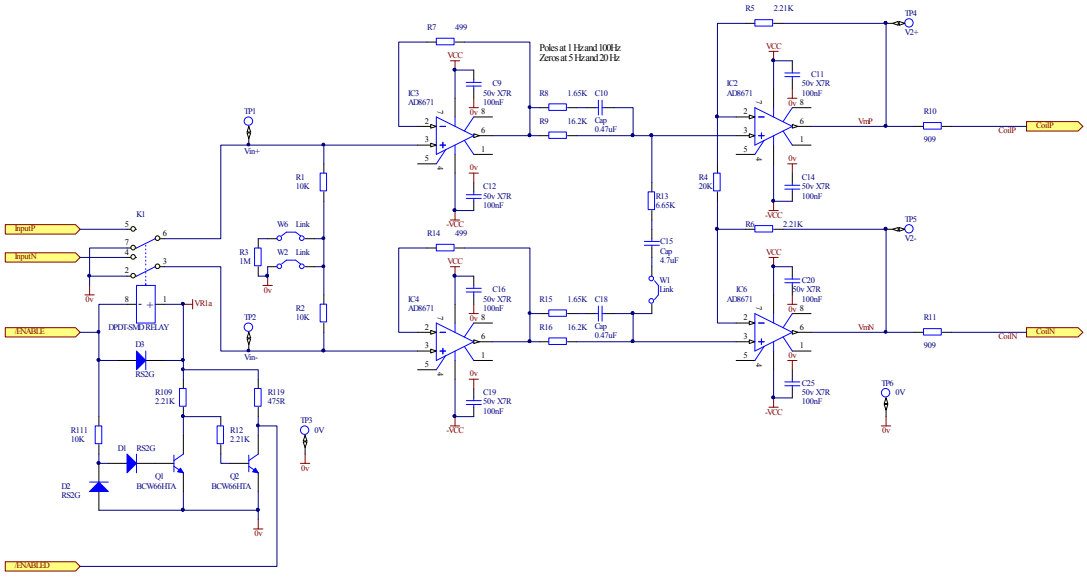

Figure 2: AdL Low Current Coil Driver Circuit

As can be seen from the schematic, the response of each of the four driver channels has poles at 1Hz and 100Hz and zeros at 5Hz and 20Hz. The figure below shows the response of a single channel from voltage in to current out where the output load is the nominal 20 ohms of the LIGO OSEM coil used for the middle stage of the suspension.

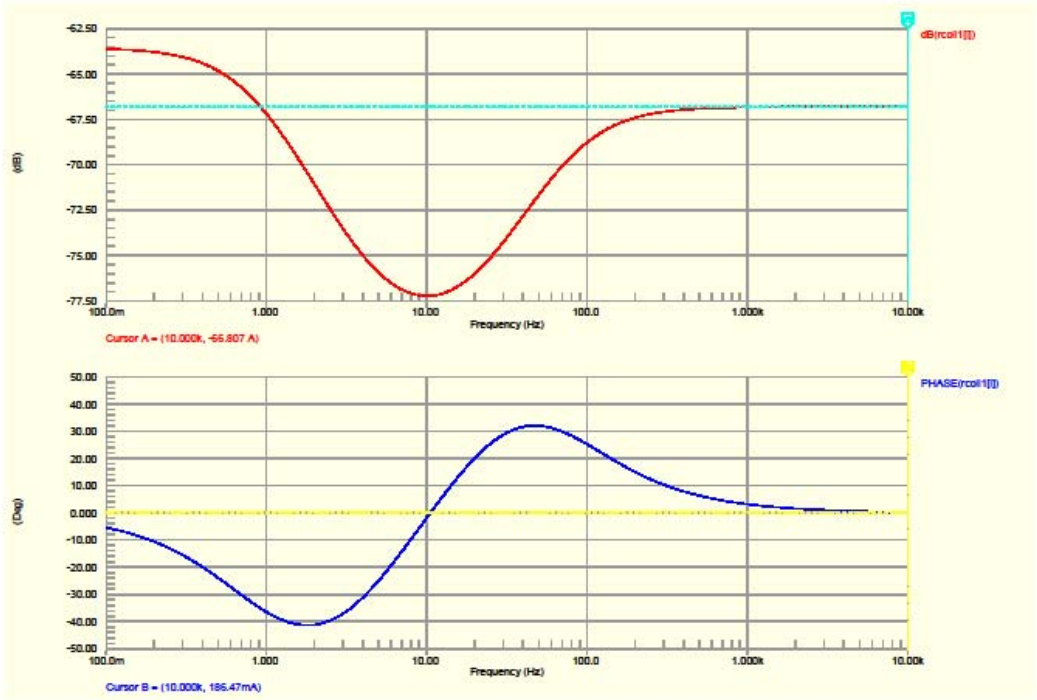

Figure 3: Driver Response, Voltage IN to Current OUT

The response of the driver was tailored to meet both the dynamic range and noise requirements without the need for mode switching. In addition to considering the design in the context of the

driver only, the actual dynamic range and output noise of the AdL DACs (General Satndards model number PCIe-16AO16) has been taken into account. This consideration is the main reason that the poles and zeros have been added to the design. The sections below detail how the design meets each of the requirements.

3.1 Dynamic Range

The driver must be capable of providing $3mA_{peak}$ for frequencies less than 1KHz. The dynamic range of the DACs used to provide the input for the drivers is $10V_{peak}$. The figure below shows the output current versus frequency for $10V_{peak}$ inputs. The same information can be obtained from Figure 3 above by converting to a linear scale and multiplying by 10.

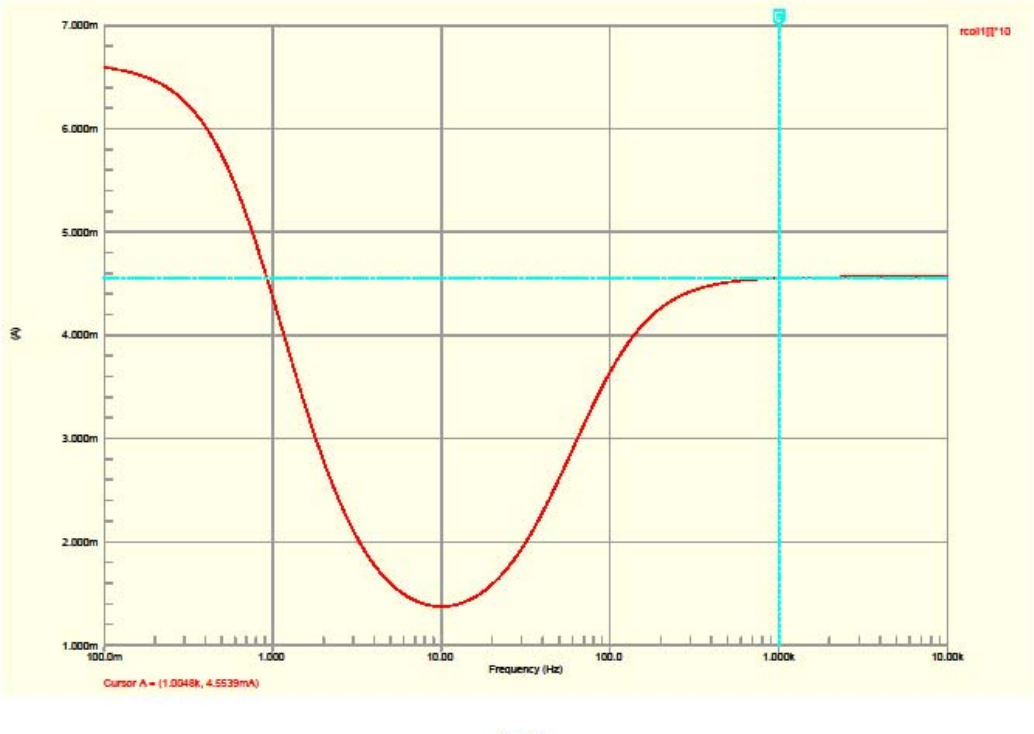

Figure 4: Coil Current vs. Freq for 10V input

Note that the design meets the output current requirement for 65Hz<freq<1KHz and for frequencies below 1.8Hz. The reason that the design cannot meet the range requirement for all frequencies is due to the output noise of the DACs. This noise and the necessary filtering are discussed in the section below.

3.2 Noise

The noise requirement for the driver, less than 125pA/√Hz, for 10Hz<freq<15Hz, is not particularly challenging if the driver is considered by itself. It is when the DAC that provides the input signal to the driver is considered that things get interesting. Tests conducted at CIT on the General Standards DAC module have shown that the output-referred noise is approximately 700nV/√Hz and the dynamic range of the output is $10V_{peak}$. This leads to a dynamic range over output noise of:

$$FOM_{DAC} = 10Vpeak/700nV/\sqrt{Hz} = 143\ dB$$

The dynamic range over the noise requirement at 10Hz is:

$$FOM_{req} = 3mApeak/125pAV/\sqrt{Hz} = 148\ dB$$

This means that regardless of the filtering applied to the DAC signal, the dynamic range and noise requirements cannot be simultaneously met. The design chosen for the driver meets the dynamic range requirements for frequencies below 1.8Hz and above 63Hz, but falls approximately a factor of two short at 10Hz. If it is later determined that the requirements for noise or dynamic range can be relaxed, or a better DAC is chosen, there should be enough flexibility in the circuit design to accommodate changes with only component value adjustments. The plot below shows the output noise current versus frequency for a white input noise voltage of 700nV/√Hz. Note that the output-referred noise current at 10Hz is 96pAV/√Hz.

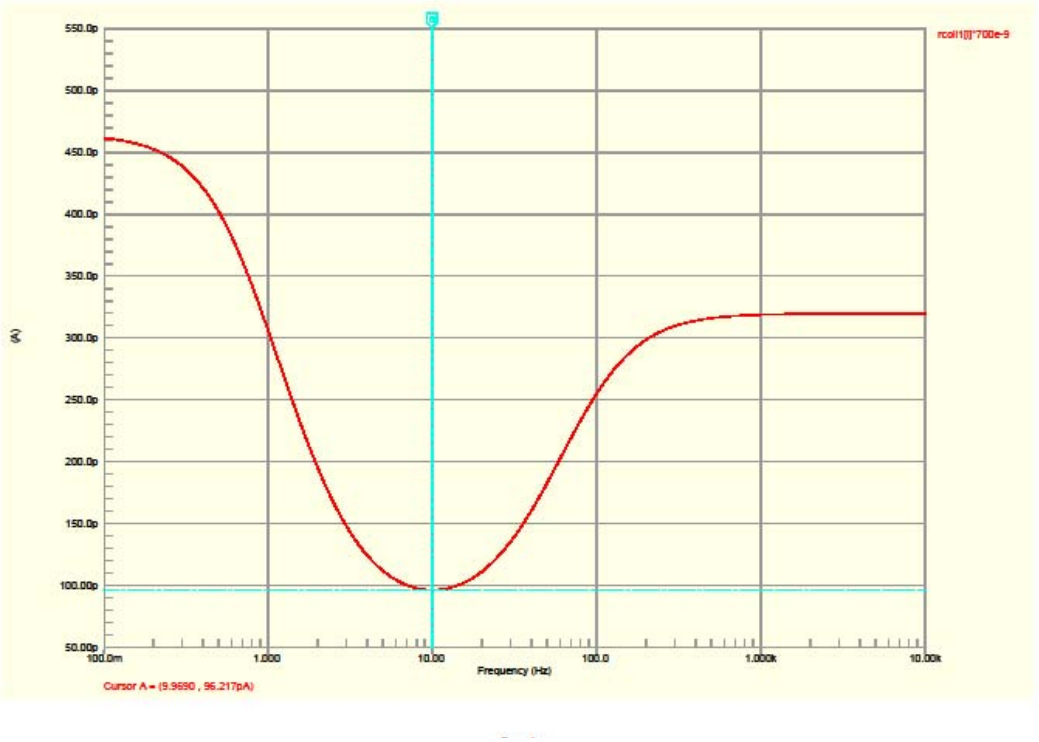

Figure 5: Output Noise Current for White 700nV/√Hz Source

For reference, the figure below shows the output noise current for the coil driver alone. Note that at 10Hz the output noise current from the driver is 10pAV/√Hz.

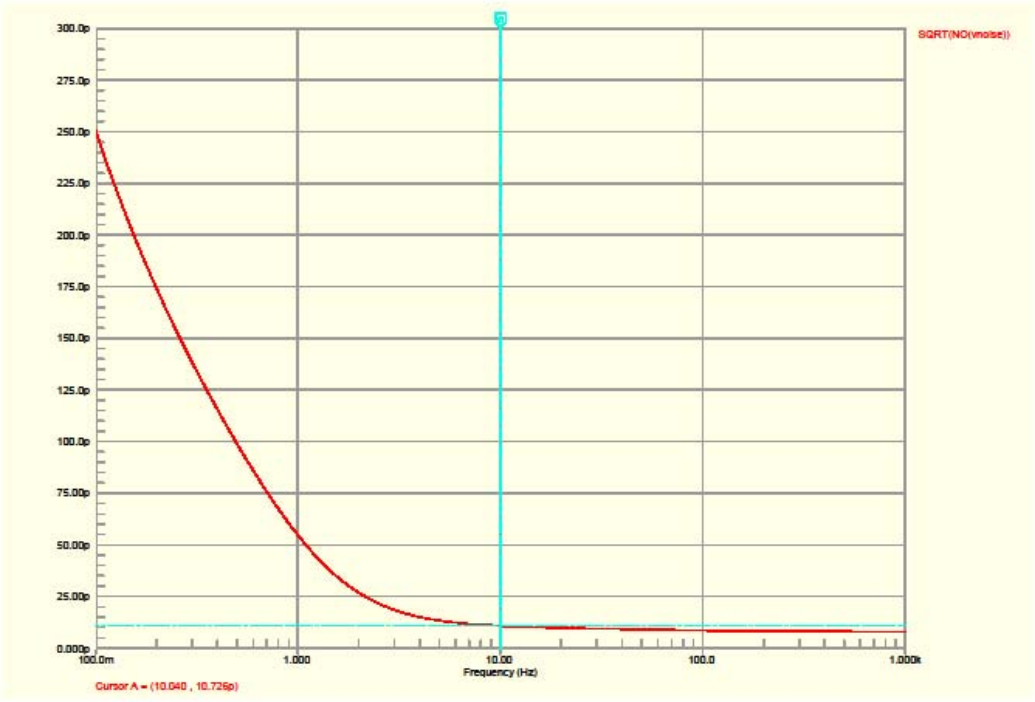

Figure 6: Driver Only Output Noise

4 Prototype Test Results

A four channel prototype of driver was fabricated and tested. The circuit diagram for the board is LIGO document D0900884-v1. The test plan used for the evaluation is LIGO document T0900190-v1. The prototype was fabricated in the format needed for AdL and is compatible with the standard noise monitor board being used by the UK in the quad designs. Additionally, all components used are readily available in the US and UK or have equivalents that can be obtained. The figures below show the prototype board mounted in a standard LIGO 1U chassis along with the monitor board and wiring harnesses.

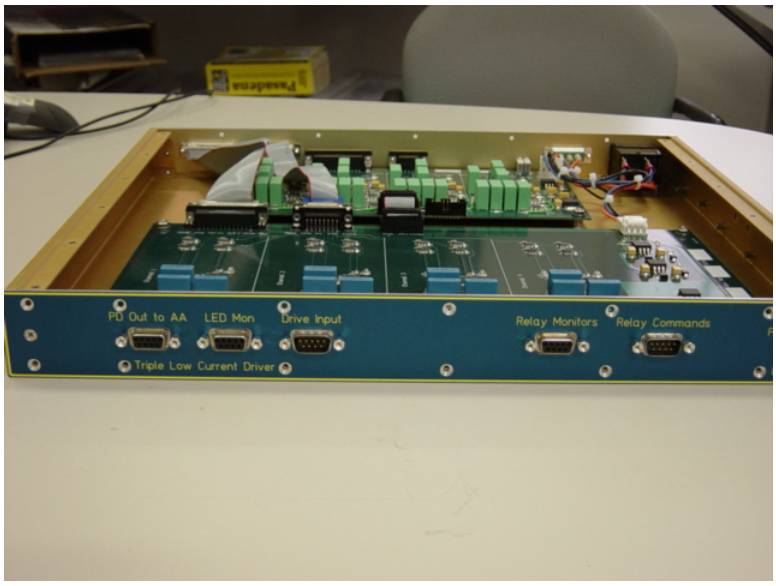

Figure 7: Low Current Driver Front View

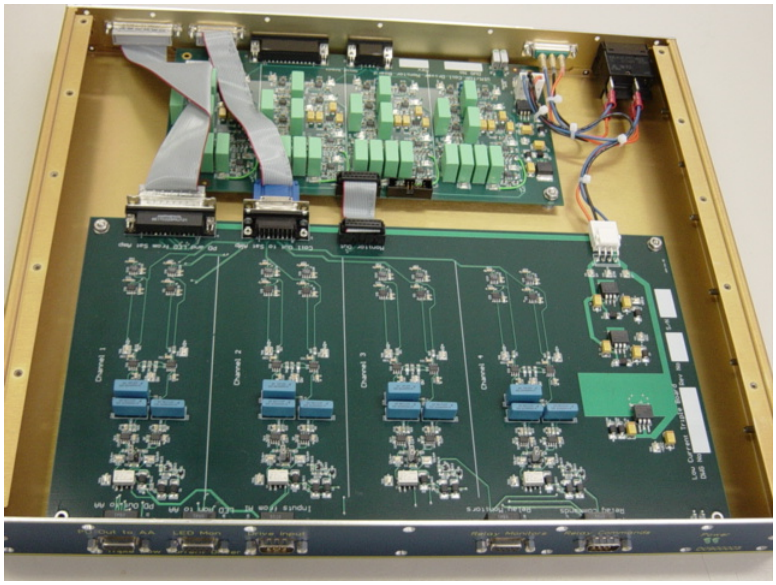

Figure 8: Low Current Driver Top View

Figure 9: Low Current Driver Rear View

4.1 Coil Driver Response

The figures below show the measured magnitude and phase response as compared to the simulation.

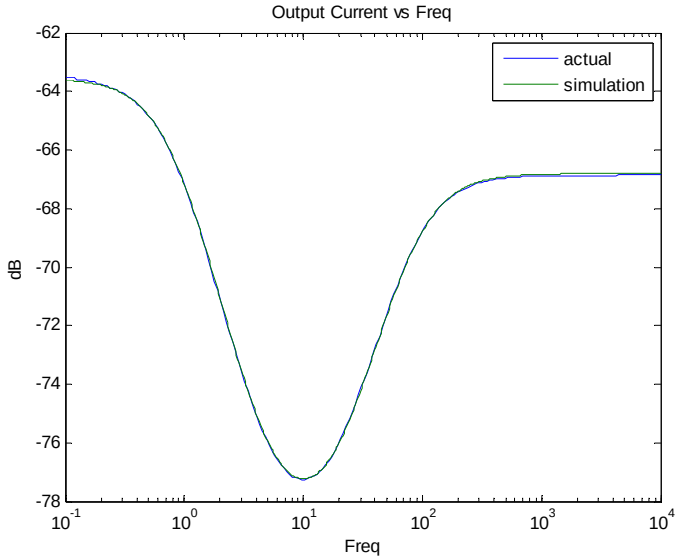

Figure 10: Magnitude Response Actual vs Simulation

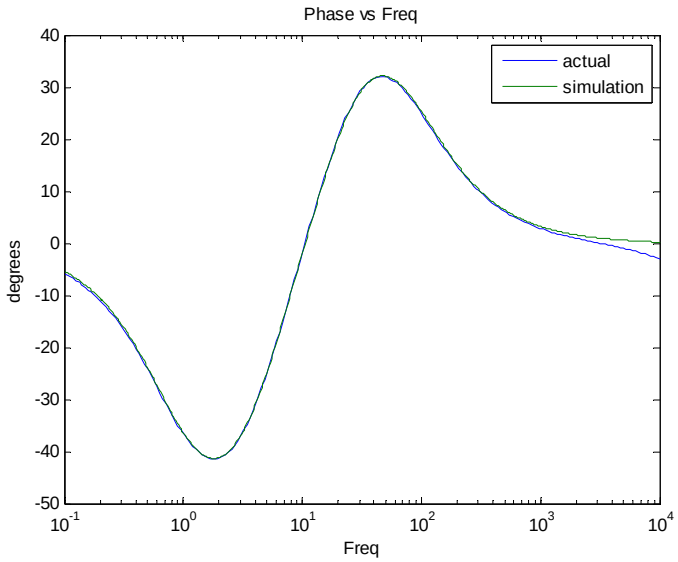

Figure 11: Phase Response Actual vs Simulation

As can be seen from the figures above the actual response of the driver matches the simulation very closely. The small deviation in phase above 1KHz is caused by the response of the differential driver used in the test setup. As part of the testing the maximum required output current was confirmed using a 1KHz sine wave. During this testing no overheating of components or other problems were observed.

4.2 Output Noise

The output noise of the driver was measured according to the test plan. As it is very difficult to measure noise current directly, the output noise voltage of the driver was measured and compared to the simulation and the requirements. As was described in section 3.2 above, the predicted output noise of the driver is far below what is required. The actual output noise was measured and compared to the simulation. The simulation predicts that the output voltage noise of the driver should be approximately 19nV/√Hz. The measured output noise for all channels of the driver was 20nV/√Hz. Note that 19nV/√Hz corresponds to approximately 11pA/√Hz which is a factor of 10 below the requirement.

4.3 Other Monitors and Circuitry

4.3.1 Noise, Output Voltage and Current Monitors

The low current driver board has been designed to operate with the UK standard noise monitor board. This board provides low noise monitors, fast current monitors and RMS current monitors for each channel. The input-referred noise of the noise monitor circuitry is compatible with the output noise voltage of the driver.

4.3.2 Relay Enables and Status

Each channel of the driver has an enable relay on the input. This relay is a normally open relay and must be provided a driver signal to enable each channel. If the relay is not energized, the inputs to each channel are tied to circuit ground. The status of each relay can be monitored through circuitry provided in the design.

4.3.3 PD and LED Signal Pass Through

The design of the driver board is compatible with both the UK and US satellite amplifiers used in the AdL suspension system. This compatibility requires that the PD and LED signals from the satellite amplifiers be passed through the drivers and made available to the AdL control system. Additionally, the power for the satellite amplifiers must be provided by the driver. Signal continuity for the PD and LED signals and power on the appropriate pins of the satellite amplifier interface connector was confirmed during the testing.

5 Status

Only a few minor changes to the circuit boards were necessary during the prototyping phase. They were:

- TP3 needs to be labeled as a return for each channel
- The diode footprint for the RS2G diodes needs to be changed from SMC to SMB
- Link W1 was added to each channel to provide a convenient means of disabling the dewhitening filter on each channel.

Presently there are 4 boards that can be used in the recycling mirror test stand and as spares for the AdL. One of these boards is mounted in a chassis with a monitor board, but chassis and front and rear panels exist for all 4.

Once the changes above are made to artwork, the full Altium design package for the project will be made available to the UK. The cross referenced UK part numbers for all components needs to be confirmed on the final bill of materials prior to procurement of components.

A test plan (T0900190-v1) exists for the board and was used during prototyping to verify operation.