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Laser Interferometer Gravitational Wave Observatory (LIGO) Project

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Timing Slave Description

D070071-B

Basic Ideas:

The timing slave drawn in D070071 is the successor of the D050093 and D050442. It implements a Xilinx Spartan 3 1600E FPGA instead of the discrete logic of the previous models. However, it can implement exactly the same protocol and clock synchronization as the previous models, but with the potential to add additional features and diagnostics later. The new timing slave is also a two board design. D070071 uses two Samtec QSE-040 high density header connectors (mates with Samtec QTE-040) which connects to a daughter board. The two Samtec connectors allow for 64 LVDS pairs or 128 2.5V CMOS logic lines which can be configured in either direction. This allows the easy development of daughter boards to interface any standard.

Circuit Description:

The timing slave requires a single +12 V digital supply. It internally generates a +3.3 V rail which is used to generate secondary +1.2 V for the FPGA core voltage, +2.5 V for the FPGA IO voltage and +1.8 V for the configuration flash PROM. It also generates a +10 V for the analog PLL circuit. The +12 V, +3.3 V and +2.5 V supplies are made available to the daughter board. The maximum currents are 2 A, 4 A and 0.5 A, respectively.

The timing signal is distributed over fibers. The timing slave uses standard SFP modules which need to be loaded with 100 baseFX or OC3 fiber transceivers. For example, the Avago HFBR-57E0 can be used for multi-mode LC fiber cables, whereas the Avago AFCT-5760 can be used for single-mode LC fiber cables. The transceiver signals are routed to the FPGA as LVDS.

A phase detector made from two flip-flops and a NAND gate generates the PLL error signal which is amplified and filtered before it is sent to the local VCXO. The local VCXO runs at 2^{26} Hz and serves as the main clock to the FPGA. The two flip-flops are also fed through the FPGA. One of the signals is the VCXO clock divided by 8. The other signal is fed from the fiber receiver. The loop shape is given by two poles at 0 Hz and a zero at 34 Hz. The nominal unity gain frequency is 50 Hz. An ADC which is read by the FPGA is used to monitor the control voltage to the VCXO and to diagnose when the VCXO runs out of range due to aging.

A flash PROM is used to program the FPGA during startup. The JTAG chain of the flash PROM as well as the FPGA are made available through a frond panel header connector. The JTAG port can be used to reprogram the timing slave. An SMD LED indicates that the FPGA program has been loaded. The push-button can be used to reload the program.

The two LEDs on the front indicate the availability of the +3.3V supply and the status of the fiber receiver. When off, no signal is received. When continuously on, a signal is received but synchronization has not been achieved. Turning on and off every second indicates a fully working and synchronized receiver. A DIP switch is used to help configuration; details to be determined.

Daughter Board:

A daughter board template is available under D070072-B. Each daughter board should implement a EEPROM which contains the board identification and configuration information. The daughter board can also insert itself into the JTAG chain, but R1 on the timing slave has to be removed first.

The daughter board connectors are Samtec QTE-040-03-L-D-A for a board-to-board spacing of 11 mm. The pin-out of the daughter board connectors are listed in the Appendix. All pins can be used as inputs or outputs. Global clock pins are available on signals S1, S16, S33 and S48. Pins S8, S9, S24 and S25 feed clock inputs for the left-hand side, whereas S40, S41, S56 and S57 feed clock inputs for the right-hand side.

The serial clock, chip select, serial in and serial out signals for the EEPROM are available through CFG_CLK, CFG_CS, CFG_SI and CFG_SO, respectively. SW9 and SW10 are extensions of the DIP switch and are internally pulled high. SW9 should always be connected to GND to indicate that a daughter board is present. SW10 can be used as needed.

Connector		XC3S1600E-4FG320C			
Signal	P1	Name	Pin	Bank	IO
TMS	2				
TDO	4				
GND	6				
GND	8				
S1_P	10	L14P_0/GCLK10	C9	0	CLK
S1_N	12	L14N_0/GCLK11	D9	0	CLK
S2_N	14	L02N_3	D2	3	IO
S2_P	16	L02P_3	D1	3	IO
S3_P	18	L03P_3	E2	3	IO
S3_N	20	L03N_3	E1	3	IO
S4_N	22	L05N_3	F2	3	IO
S4_P	24	L05P_3	F1	3	IO
S5_P	26	L10P_3	H2	3	IO
S5_N	28	L10N_3	H1	3	IO
S6_N	30	L08N_3	H5	3	IO
S6_P	32	L08P_3	H6	3	IO
S7_P	34	L15P_3	L1	3	IO
S7_N	36	L15N_3	L2	3	IO
S8_N	38	L13N_3/LHCLK5	K4	3	CLK
S8_P	40	L13P_3/LHCLK4	K3	3	CLK
S9_P	42	L14P_3/LHCLK6	K6	3	CLK
S9_N	44	L14N_3/LHCLK7	K5	3	CLK
S10_N	46	L21N_3	P1	3	IO
S10_P	48	L21P_3	P2	3	IO
S11_P	50	L23P_3	R3	3	IO
S11_N	52	L23N_3	R2	3	IO
S12_N	54	L24N_3	T1	3	IO
S12_P	56	L24P_3	T2	3	IO
S13_P	58	L22P_3	P3	3	IO
S13_N	60	L22N_3	P4	3	IO
S14_N	62	L07N_2	P7	2	IO
S14_P	64	L07P_2	N7	2	IO
S15_P	66	L06P_2	V5	2	IO
S15_N	68	L06N_2	V6	2	IO
S16_N	70	L13N_2/GCLK15	V9	2	CLK
S16_P	72	L13P_2/GCLK14	U9	2	CLK
GND	74				
GND	76				
CFG_SI	78	L04N_2	T5	2	O
CFG_CS	80	IO	U5	2	O

Connector		XC3S1600E-4FG320C			
Signal	P1	Name	Pin	Bank	IO
TCK	1				
TDI	3				
SW9	5	IO	C4	0	I
SW10	7	L23N_0	D5	0	I
S17_P	9	L18P_0	C7	0	IO
S17_N	11	L18N_0	D7	0	IO
S18_N	13	L04N_3	E3	3	IO
S18_P	15	L04P_3	E4	3	IO
S19_P	17	L19P_0	F7	0	IO
S19_N	19	L19N_0	E7	0	IO
S20_N	21	L06N_3	G4	3	IO
S20_P	23	L06P_3	G3	3	IO
S21_P	25	L07P_3	G6	3	IO
S21_N	27	L07N_3	G5	3	IO
S22_N	29	L09N_3	H3	3	IO
S22_P	31	L09P_3	H4	3	IO
S23_P	33	L17P_3	L6	3	IO
S23_N	35	L17N_3	L5	3	IO
S24_N	37	L11N_3/LHCLK1	J4	3	CLK
S24_P	39	L11P_3/LHCLK0	J5	3	CLK
S25_P	41	L12P_3/LHCLK2	J1	3	CLK
S25_N	43	L12N_3/LHCLK3	J2	3	CLK
S26_N	45	L16N_3	L4	3	IO
S26_P	47	L16P_3	L3	3	IO
S27_P	49	L18P_3	M4	3	IO
S27_N	51	L18N_3	M3	3	IO
S28_N	53	L19N_3	M6	3	IO
S28_P	55	L19P_3	M5	3	IO
S29_P	57	L20P_3	N4	3	IO
S29_N	59	L20N_3	N5	3	IO
S30_N	61	L05N_2	P6	2	IO
S30_P	63	L05P_2	R6	2	IO
S31_P	65	L10P_2	R8	2	IO
S31_N	67	L10N_2	T8	2	IO
S32_N	69	L09N_2	N8	2	IO
S32_P	71	L09P_2	P8	2	IO
VCCAUX	73				
VCCAUX	75				
CFG_SO	77	IP	V2	2	I
CFG_CLK	79	L04P_2	R5	2	O

Connector		XC3S1600E-4FG320C			
Signal	P2	Name	Pin	Bank	IO
VDD	1				
VDD	3				
VDD	5				
VDD	7				
S33_P	9	L11P_0/GCLK4	D10	0	CLK
S33_N	11	L11N_0/GCLK5	E10	0	CLK
S34_N	13	L19N_1	F17	1	IO
S34_P	15	L19P_1	F18	1	IO
S35_P	17	L08P_0	E11	0	IO
S35_N	19	L08N_0	F11	0	IO
S36_N	21	L16N_1	H17	1	IO
S36_P	23	L16P_1	H16	1	IO
S37_P	25	L15P_1	J13	1	IO
S37_N	27	L15N_1	J12	1	IO
S38_N	29	L09N_1	L15	1	IO
S38_P	31	L09P_1	L16	1	IO
S39_P	33	L10P_1	L18	1	IO
S39_N	35	L10N_1	L17	1	IO
S40_N	37	L13N_1/RHCLK5	J16	1	CLK
S40_P	39	L13P_1/RHCLK4	J17	1	CLK
S41_P	41	L12P_1/RHCLK6	J15	1	CLK
S41_N	43	L12N_1/RHCLK7	J14	1	CLK
S42_N	45	L08N_1	M18	1	IO
S42_P	47	L08P_1	N18	1	IO
S43_P	49	L18P_2	P11	2	IO
S43_N	51	L18N_2	N11	2	IO
S44_N	53	L06N_1	P18	1	IO
S44_P	55	L06P_1	P17	1	IO
S45_P	57	L02P_1	R18	1	IO
S45_N	59	L02N_1	T18	1	IO
S46_N	61	L01N_1	T17	1	IO
S46_P	63	L01P_1	U18	1	IO
S47_P	65	L03P_1	R15	1	IO
S47_N	67	L03N_1	R16	1	IO
S48_N	69	L15N_2/GCLK3	P10	2	CLK
S48_P	71	L15P_2/GCLK2	R10	2	CLK
VCCAUX	73				
VCCAUX	75				
12V	77				
12V	79				

Connector		XC3S1600E-4FG320C			
Signal	P2	Name	Pin	Bank	IO
GND	2				
GND	4				
GND	6				I
GND	8				I
S49_P	10	L09P_0	C11	0	IO
S49_N	12	L09N_0	D11	0	IO
S50_N	14	L17N_0	F8	0	IO
S50_P	16	L17P_0	E8	0	IO
S51_P	18	L03P_0	D14	0	IO
S51_N	20	L03N_0	C14	0	IO
S52_N	22	L06N_0	E12	0	IO
S52_P	24	L06P_0	F12	0	IO
S53_P	26	L15P_0	E9	0	IO
S53_N	28	L15N_0	F9	0	IO
S54_N	30	L20N_1	G13	1	IO
S54_P	32	L20P_1	G14	1	IO
S55_P	34	L17P_1	H14	1	IO
S55_N	36	L17N_1	H15	1	IO
S56_N	38	L11N_1/RHCLK1	K12	1	CLK
S56_P	40	L11P_1/RHCLK0	K13	1	CLK
S57_P	42	L12P_1/RHCLK2	K15	1	CLK
S57_N	44	L12N_1/RHCLK3	K14	1	CLK
S58_N	46	L05N_0	B13	0	IO
S58_P	48	L05P_0	A13	0	IO
S59_P	50	L07P_1	M15	1	IO
S59_N	52	L07N_1	M16	1	IO
S60_N	54	L05N_1	M13	1	IO
S60_P	56	L05P_1	M14	1	IO
S61_P	58	L04P_1	N15	1	IO
S61_N	60	L04N_1	N14	1	IO
S62_N	62	L21N_2	P12	2	IO
S62_P	64	L21P_2	N12	2	IO
S63_P	66	L22P_2	P13	2	IO
S63_N	68	L22N_2	R13	2	IO
S64_N	70	L24N_2	R14	2	IO
S64_P	72	L24P_2	T14	2	IO
GND	74				
GND	76				
GND	78				
GND	80				