# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P84.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

Drive Card ID.....T\_ACQ84..... Monitor Card ID....Mon250.....

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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P84.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P84.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P84	Serial No	
Test Engineer	.Xen	-		
	4710140			

Date.....17/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P84.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P84	Serial No
Test Engineer	.Xen	
Date	17/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P84	Serial No
Test Engineer	.Xen	
Date	.17/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.77	2.9µV√Hz	$\checkmark$
2		1.57	2.9µV√Hz	$\checkmark$
3		1.61	2.9µV√Hz	$\checkmark$
4		1.66	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P84	Serial No
Test Engineer	.Xen	
Date	.17/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P84.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ F	P84	Serial No
Test EngineerX	en		
Date17	/9/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak Io (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.122	8.6mA	>2.5mA peak	$\checkmark$
Ch4	0.124	8.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.236	16.7mA	>2.5mA peak	$\checkmark$
Ch4	0.238	16.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit1	L_ACQ_	P84	.Serial No
Test Engineer>	Ken	• • • • • • • • • • • • • • • • • • • •	
Date1	7/9/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T ACQ P84	Serial No
Test Engineer	.Xen	
Date	.17/9/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch2	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch3	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch4	-143.5	-91.7	-151.7	26.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ84P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TASCQ48P
Driver board ID	TASCQ48P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON250
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

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LIGO- T0900xxxx

Advanced LIGO UK

March 2010

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID......T\_ACQ1..... Monitor Card ID....Mon183.....

### Contents

- 1 Description
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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P1.....Serial No..... Test Engineer....Xen.... Date......19/10/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	T ACQ F	P1Serial No
Test Engineer.	Xen	
Date	14/10/10.	

# 3. Inspection

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P1	Serial No
Test Engineer.	Xen	
Date	14/10/10	
Date	14/10/10	

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

# PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{v}}$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P1Serial No
Test Engineer	Xen	
Date		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P1	Serial No
Test Engineer	.Xen	
Date	.14/10/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.60	2.9µV√Hz	$\checkmark$
2		1.85	2.9µV√Hz	$\checkmark$
3		1.43	2.9µV√Hz	$\checkmark$
4		1.00	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P1	Serial No
Test Engineer	.Xen	
Date	.14/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specificatio (Vo/20) x 1.414		Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P1	Serial No
Test EngineerX	en	
Date1	9/10/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	9.0mA >2.5mA peak	
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P1	Serial No
Test Engineer	Xen	
Date	19/10/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	140.7mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T ACQ P1	Serial No
Test Engineer	.Xen	
Date	.14/10/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch3	-143.5	-89.3	-149.3	34.3	$\checkmark$
Ch4	-143.5	-92.7	-152.7	23.2	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....Serial No ..... Test Engineer ..... Date .....

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.
- 2. Unplug all external connections.

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.

4. Check that all internal connectors are firmly mated.

5. Tighten the screw-locks holding all the external connectors.

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.

8. Check that all links W4 and W2 are in place.

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	
Driver board ID	
Driver board Drawing No/Issue No	
Driver board Serial Number	
Monitor board ID	
Monitor board Drawing No/Issue No	
Monitor board Serial Number	

10. Check the security of any modification wires.

11. Visually inspect.

12. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P2.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

Drive Card ID.....T\_ACQ2P..... Monitor Card ID...Mon137.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P2.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P2.....Serial No..... Test Engineer....Xen.... Date......20/5/10.....

### **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P2	Serial No
Test Engin	eerXen	
Date	20/5/10	

Date......20/5/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

### 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P2.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P2	Serial No
Test Engineer	Xen	
Date	20/5/10	

### 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

### **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

### **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

### **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P2	Serial No
Test Engineer	Xen	
Date	.20/5/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.66	2.9µV√Hz	$\checkmark$
2		0.94	2.9µV√Hz	$\checkmark$
3		1.43	2.9µV√Hz	$\checkmark$
4		0.92	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P2	Serial No
Test Engineer	Xen	
Date	.20/5/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P2.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch2	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch3	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch4	64.5mV	3.2mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P2	.Serial No
Test Engineer	Xen	
Date	20/5/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.133	9.4mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.250	17.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

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Test EngineerXen	 ۱	
Date20/5	5/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

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### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch2	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch3	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch4	-143.5	-91.5	-151.5	26.6	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....Serial No ..... Test Engineer ..... Date .....

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis. N/A

7. Check that all the LEDs are nicely centred.  $\checkmark$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number.  $\sqrt{Record}$  below:

UoB box ID	TACQ2 P
Driver board ID	TACQ2
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ2
Monitor board ID	MON137
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON137 P

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm

### TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P3.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

Drive Card ID.....T\_ACQ3P..... Monitor Card ID...Mon136.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

### **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P3.....Serial No..... Test Engineer....Xen.... Date......20/5/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

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### **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

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# 1. Continuity Chooks

### **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

### 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P3.....Serial No..... Test Engineer....Xen.... Date......19/5/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P3Serial No	
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Date			

### 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

### FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

### **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

### **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

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### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.97	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.97	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.14	2.9µV√Hz	$\checkmark$
2		0.92	2.9µV√Hz	$\checkmark$
3		1.20	2.9µV√Hz	$\checkmark$
4		1.48	2.9µV√Hz	$\checkmark$

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Date	.3/6/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

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#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	65mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch3	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T_ACQ_P3	Serial No
Test Engineer	Xen	
Date	.20/5/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	12mV	600uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	130mV	9.2mA	>2.5mA peak	$\checkmark$
Ch2	130mV	9.2mA	>2.5mA peak	$\checkmark$
Ch3	130mV	9.2mA	>2.5mA peak	$\checkmark$
Ch4	125mV	8.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.240	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P3	Serial No
Test EngineerXe	n	
Date20/	5/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P3	Serial No
Test Engineer	.Xen	
Date	.20/5/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dBV√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.1	-151.1	27.9	$\checkmark$
Ch2	-143.5	-90.7	-150.7	29.2	$\checkmark$
Ch3	-143.5	-90.5	-150.5	29.9	$\checkmark$
Ch4	-143.5	-91.1	-151.1	27.9	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TAQ3.....Serial No ..... Test Engineer ... RMC Date ......9/6/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\checkmark$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TAQ3 P
Driver board ID	TAQ3
Driver board Drawing No/Issue No	D0901047_P
Driver board Serial Number	TAQ3
Monitor board ID	MON136
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON136

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm

### TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID......T\_ACQ4P..... Monitor Card ID.....Mon134....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

### **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P4.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P4.....Serial No..... Test Engineer....Xen.... Date......18/5/10.....

### **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit1	Г_ACQ_P4	Serial No
Test Engineer>	Ken	
Date1	8/5/10	

# 4. Continuity Chacks

### **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+ 4		$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL			To J1 PIN	OK?
1	Imon1P			5	$\checkmark$
2	Imon2P			6	$\checkmark$
3	Imon3P			7	$\checkmark$
4	Imon4P			8	$\checkmark$
	5	0V		$\checkmark$	
6	Imon1N			18	$\checkmark$
7	Imon2N			19	$\checkmark$
8	Imon3N	20		$\overline{\mathbf{v}}$	
9	Imon4N			21	$\overline{\mathbf{v}}$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

### 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P4.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P4	Serial No
Test Engineer	Xen	
Date	.18/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indie	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P4	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.90	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.88	2.9µV√Hz	$\checkmark$
2		0.88	2.9µV√Hz	$\checkmark$
3		1.28	2.9µV√Hz	$\checkmark$
4		1.87	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P4	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P4.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	66.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	66.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	66.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	66.5mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	Г АСQ Р4	Serial No
Test Engineer>	Ken	
Date1	8/5/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.122	8.6mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.235	16.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P4	Serial No
Test EngineerXe	n	
Date18/	5/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P4	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch3	-143.5	-94.1	-154.1	19.7	$\checkmark$
Ch4	-143.5	-92.1	-152.1	24.8	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ4 P.....Serial No ..... Test Engineer ......RMC Date ......9/6/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ4 P
Driver board ID	TACQ4 P
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ4 P
Monitor board ID	MON134
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON134

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ11P..... Monitor Card ID...Mon135.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
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- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P5.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P5.....Serial No..... Test Engineer....Xen.... Date......18/5/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ P5	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

**4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

# PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+ 4		$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\overline{\mathbf{A}}$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P5.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P5	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indie	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P5	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.03	2.9µV√Hz	$\checkmark$
2		2.12	2.9µV√Hz	$\checkmark$
3		0.94	2.9µV√Hz	$\checkmark$
4		0.95	2.9µV√Hz	$\checkmark$

Unit	.T_ACQ_P5	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P5.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	64.5mV	3.2mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch3	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.320	22.6mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P5	Serial No
Test Engineer	Xen	
Date	18/5/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.240	17.0mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.248	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P5	Serial No
Test EngineerXer	n	
Date18/	5/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P5	Serial No
Test Engineer	.Xen	
Date	.18/5/10	

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-90.4	-150.4	30.2	$\checkmark$
Ch3	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch4	-143.5	-92.0	-152.0	25.1	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TACQ5.....Serial No ..... Test Engineer ......RMC Date ......9/6/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ5 P
Driver board ID	TACQ5
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ5
Monitor board ID	MON135
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON135

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ6P..... Monitor Card ID...Mon133.....

### Contents

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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P6.....Serial No..... Test Engineer....Xen.... Date......18/5/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P6.....Serial No..... Test Engineer....Xen.... Date......17/5/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P6	Serial No
Test Engin	eer <mark>Xe</mark> n	
Date	17/5/10	

Date.....17/5/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+ 4		$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P6	Serial No
Test Engineer	.Xen	
Date	.17/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indie	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P6	Serial No
Test Engineer	.Xen	
Date	.17/5/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.93	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.53	2.9µV√Hz	$\checkmark$
2		1.06	2.9µV√Hz	$\checkmark$
3		1.38	2.9µV√Hz	$\checkmark$
4		1.38	2.9µV√Hz	$\checkmark$

Unit	.T_ACQ_P6	Serial No
Test Engineer	Xen	
Date	.3/6/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	65mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch2	0.064	4.6mA	>2.5mA peak	$\checkmark$
Ch3	0.064	4.6mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.6mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
Unit	.T ACQ P6	Serial No		
---------------	-----------	-----------		
Test Engineer	.Xen			
Date	3/6/10			

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

#### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P6	Serial No
Test EngineerX	en	
Date3/	/6/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P6	Serial No
Test Engineer	.Xen	
Date	.3/6/10	

#### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dBV√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-88.7	-148.7	36.7	$\checkmark$
Ch2	-143.5	-91.1	-151.1	27.9	$\checkmark$
Ch3	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch4	-143.5	-92.1	-152.1	24.8	$\checkmark$

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ6 P....Serial No .... Test Engineer ......RMC Date ......9/6/10

#### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ6 P
Driver board ID	TACQ6
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ6
Monitor board ID	MON133
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON133

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ11P..... Monitor Card ID...Mon132.....

#### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

### **Block diagram**



#### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit.......T\_ACQ\_P7.....Serial No..... Test Engineer....Xen.... Date......17/5/10....

#### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	.T ACQ P7	Serial No
Test Engineer	.Xen	
Date	.17/5/10	

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P7	Serial No
Test Engin	eer <mark>Xe</mark> n	
Date	17/5/10	

Date.....17/5/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

#### **LED Mon**

PIN	SIGNAL			To J1 PIN	OK?
1	Imon1P			5	$\checkmark$
2	Imon2P			6	$\checkmark$
3	Imon3P			7	$\checkmark$
4	Imon4P			8	$\checkmark$
	5	0V		$\checkmark$	
6	Imon1N			18	$\checkmark$
7	Imon2N			19	$\checkmark$
8	Imon3N			20	$\checkmark$
9	Imon4N			21	$\overline{\mathbf{v}}$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

#### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P7	Serial No
Test Engineer	.Xen	
Date	.17/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

### **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P7	Serial No
Test Engineer	Xen	
Date	.17/5/10	

#### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

#### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

#### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for CH2.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give  $2.9\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.14	2.9µV√Hz	$\checkmark$
2		1.69	2.9µV√Hz	$\checkmark$
3		1.66	2.9µV√Hz	$\checkmark$
4		1.85	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P7	Serial No
Test Engineer	Xen	
Date	.17/5/10	

#### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	64.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	64.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	64.5mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	64.5mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch3	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.320	22.6mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.320	22.6mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P7	Serial No
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Date	17/5/10	

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak Io (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

#### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	127mV	9.0mA	>2.5mA peak	$\checkmark$
Ch2	128mV	9.0mA >2.5mA peak		$\checkmark$
Ch3	131mV	9.3mA	>2.5mA peak	$\checkmark$
Ch4	130mV	9.2mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specificatio (Vo/20) x 1.414		Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P7	Serial No
Test Engineer	Xen	
Date	17/5/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P7	Serial No
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Date	.17/5/10	

#### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-90.6	-150.6	31.6	$\checkmark$
Ch2	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-92.0	-152.0	25.1	$\checkmark$

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TACQ7 P.....Serial No ..... Test Engineer .....RMC Date ......10/6/10

#### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number.  $\sqrt{\text{Record below}}$ :

UoB box ID	TACQ7P
Driver board ID	TACQ7
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ7
Monitor board ID	MON132
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON132

10. Check the security of any modification wires. None

11. Visually inspect. . √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID......T\_ACQ8P..... Monitor Card ID.....Mon131....

#### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
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# **1. Description**

### **Block diagram**



#### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P8.....Serial No..... Test Engineer....Xen.... Date......14/5/10....

#### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P8.....Serial No..... Test Engineer....Xen.... Date......14/5/10.....

# **3. Inspection**

#### Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

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# 4. Continuity Obsolve

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

#### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

#### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

#### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P8	Serial No
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Date	.14/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

### **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P8	Serial No
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#### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

#### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.89	2	1.86v r.m.s	$\checkmark$
2	1.89	5	1.86v r.m.s	$\checkmark$
3	1.89	8	1.86v r.m.s	$\checkmark$
4	1.89	11	1.86v r.m.s	

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	1	1.86v dc	$\checkmark$
2	1.93	4	1.86v dc	$\checkmark$
3	1.93	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

#### 8.4 Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give  $2.9\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.67	2.9µV√Hz	$\checkmark$
2		1.25	2.9µV√Hz	$\checkmark$
3		2.69	2.9µV√Hz	$\checkmark$
4		1.72	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P8	Serial No
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Date	.14/5/10	

#### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	66mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	66mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	66mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	66mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.393	27.8mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.393	27.8mA	>2.5mA peak	$\checkmark$
Ch4	0.393	27.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.418	29.6mA	>2.5mA peak	$\checkmark$
Ch2	0.418	29.6mA	>2.5mA peak	$\checkmark$
Ch3	0.418	29.6mA	>2.5mA peak	$\checkmark$
Ch4	0.418	29.6mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P8	Serial No
Test Engineer	Xen	
Date	14/5/10	

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

#### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.373	26.4mA	>2.5mA peak	$\checkmark$
Ch2	0.373	26.4mA	>2.5mA peak	$\checkmark$
Ch3	0.372	26.3mA	>2.5mA peak	$\checkmark$
Ch4	0.373	26.4mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P8	Serial No
Test EngineerX	en	
Date14	4/5/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P8	Serial No
Test Engineer	.Xen	
Date	.14/5/10	

#### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch2	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch3	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch4	-143.5	-90.5	-150.5	29.9	

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TACQ8 P.....Serial No ..... Test Engineer ......RMC Date ......10/6/10

#### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box. .  $\checkmark$ 

4. Check that all internal connectors are firmly mated. .  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number.  $\sqrt{\text{Record below}}$ :

UoB box ID	TACQ8
Driver board ID	TACQ8 P
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ8
Monitor board ID	MON131
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON131

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ9P..... Monitor Card ID...Mon130.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P9.....Serial No..... Test Engineer....Xen.... Date......14/5/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_P9	Serial No
Test Engineer	Xen	
Date	.14/5/10	

# 1. Continuity Chooks

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

## PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P9	Serial No
Test Engineer	.Xen	
Date	.14/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P9	Serial No
Test Engineer	.Xen	
Date	.14/5/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

## **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.89	2	1.86v r.m.s	$\checkmark$
2	1.89	5	1.86v r.m.s	$\checkmark$
3	1.89	8	1.86v r.m.s	$\checkmark$
4	1.89	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	1	1.86v dc	$\checkmark$
2	1.93	4	1.86v dc	$\checkmark$
3	1.93	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give  $2.9\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.12	2.9µV√Hz	$\checkmark$
2		1.22	2.9µV√Hz	$\checkmark$
3		1.71	2.9µV√Hz	$\checkmark$
4		1.27	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P9	Serial No
Test Engineer	.Xen	
Date	.14/5/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

## **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.326	23.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.394	27.9mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.393	27.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.418	29.6mA	>2.5mA peak	$\checkmark$
Ch2	0.418	29.6mA	>2.5mA peak	$\checkmark$
Ch3	0.417	29.5mA	>2.5mA peak	$\checkmark$
Ch4	0.418	29.6mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P9	Serial No
Test Engineer	Xen	
Date1	14/5/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.252	17.8mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.373	26.4mA	>2.5mA peak	$\checkmark$
Ch2	0.374	26.4mA	>2.5mA peak	$\checkmark$
Ch3	0.373	26.4mA	>2.5mA peak	$\checkmark$
Ch4	0.374	26.4mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P9	Serial No
Test EngineerX	en	
Date14	ŀ/5/10	

## **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P9	Serial No
Test Engineer	.Xen	
Date	.14/5/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch3	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch4	-143.5	-92.9	-152.9	22.6	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ9 P....Serial No ..... Test Engineer ......RMC Date .....10/6/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number.  $\sqrt{\text{Record below}}$ :

UoB box ID	TACQ9 P
Driver board ID	TACQ9
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ9
Monitor board ID	MON130
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON130

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ11P...... Monitor Card ID...Mon129.....

# Contents

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- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
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- 8.2 Coil Monitors
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- **10.3 Acquisition Mode**
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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit.......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......14/5/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......12/5/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. 

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL			To J1 PIN	OK?
1	Imon1P			5	$\checkmark$
2	Imon2P			6	$\checkmark$
3	Imon3P			7	$\checkmark$
4	Imon4P	8		$\checkmark$	
	5	0V		$\checkmark$	
6	Imon1N			18	$\checkmark$
7	Imon2N			19	$\checkmark$
8	Imon3N			20	$\checkmark$
9	Imon4N			21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

# Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......12/5/10.....

# 7. Relay Operation

Operate each relay in turn.

Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P10	Serial No
Test Engineer	.Xen	
Date	.12/5/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

## **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give  $2.9\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.28	2.9µV√Hz	$\checkmark$
2		1.58	2.9µV√Hz	$\checkmark$
3		1.37	2.9µV√Hz	$\checkmark$
4		1.90	2.9µV√Hz	$\checkmark$

Unit......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......13/5/10.....

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### 10.1 Noisy Mode

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch2	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch3	64.5mV	3.2mA	>2.5mA peak	$\checkmark$
Ch4	64.5mV	3.2mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch3	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.320	22.6mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......13/5/10.....

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	12mV	600uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.124	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.239	16.9mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.372	26.3mA	>2.5mA peak	$\checkmark$
Ch2	0.372	26.3mA	>2.5mA peak	$\checkmark$
Ch3	0.372	26.3mA	>2.5mA peak	$\checkmark$
Ch4	0.372	26.3mA	>2.5mA peak	$\checkmark$

Unit......T\_ACQ\_P10.....Serial No ..... Test Engineer....Xen..... Date......13/5/10.....

## **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch2	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	2.0	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.0	2.8	141.4mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch2	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-90.4	-150.4	30.2	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ10 P.....Serial No ..... Test Engineer ......RMC Date .....10/6/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number.  $\sqrt{\text{Record below}}$ :

UoB box ID	TACQ10 P
Driver board ID	TACQ10
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ10
Monitor board ID	MON129
Monitor board Drawing No/Issue No	D070480_4_K
Monitor board Serial Number	MON129

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ11P...... Monitor Card ID...Mon128.....

## Contents

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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit.......T\_ACQ\_P11.....Serial No ..... Test Engineer....Xen..... Date......12/5/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P11.....Serial No ..... Test Engineer....Xen.... Date......11/5/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed on all channels to 1nF.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P11	.Serial No .	
Test Engineer	Xen			
Date	11/5/10			

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

## PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P11	.Serial No
Test Engineer	Xen	
Date	.11/5/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P11	Serial No	
Test Engineer	Xen		
Date	11/5/10		

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	3.32	3	0.33v	$\checkmark$
2	3.31	6	0.33v	$\checkmark$
3	3.32	9	0.33v	$\checkmark$
4	3.31	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $uV/\sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain.  $10pA\sqrt{Hz}$  should give  $2.9\mu V\sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.89	2.9µV√Hz	$\checkmark$
2		1.45	2.9µV√Hz	$\checkmark$
3		1.73	2.9µV√Hz	$\checkmark$
4		1.37	2.9µV√Hz	$\checkmark$

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	65mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch3	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit.......T\_ACQ\_P11.....Serial No ..... Test Engineer....Xen..... Date......12/5/10.....

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

#### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch2	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit.......T\_ACQ\_P11.....Serial No ..... Test Engineer....Xen..... Date......12/5/10.....

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.79	139mA	>125mA peak	$\checkmark$
Ch2	1.96	2.77	139mA	>125mA peak	$\checkmark$
Ch3	1.96	2.77	139mA	>125mA peak	$\checkmark$
Ch4	1.97	2.79	139mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	156mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	156mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	156mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	156mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	156mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	163mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	156mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	163mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P11	Serial No
Test Engineer	Xen	
Date	.12/5/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V/√Hz	Measured @ 10Hz	- 60dB =	Measured in nV/√Hz	OK?
Ch1	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch4	-143.5	-90.3	-150.3	30.5	

### Notes:

Specified noise output current at 10 Hz = 10pA/root Hz (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV/ $\sqrt{Hz}$ 67 nV/ $\sqrt{Hz}$  = -143.5 dB/ $\sqrt{Hz}$  Unit.....TACQ11 P.....Serial No ..... Test Engineer ......RMC Date .....10/6/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 9mm pillars are in place in the corners of the Monitor Board towards the centre of the box.  $\checkmark$ 

4. Check that all internal connectors are firmly mated.  $\sqrt{}$ 

5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$ 

6. Check that the nuts holding the tabs of the power drivers are secure – tighten as necessary. Test with a DVM that none of the tabs are shorted to chassis.

7. Check that all the LEDs are nicely centred.  $\sqrt{}$ 

8. Check that all links W4 are in place.  $\sqrt{}$ 

9. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ11 P
Driver board ID	TACQ11
Driver board Drawing No/Issue No	D0901047_V2
Driver board Serial Number	TACQ11
Monitor board ID	MON128
Monitor board Drawing No/Issue No	D
Monitor board Serial Number	MON128

10. Check the security of any modification wires. None

11. Visually inspect. √

12. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

Drive Card ID.....T\_ACQ12..... Monitor Card ID....Mon146.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen..... Date.......6/8/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P12	Serial No
Test Engineer	Xen	
Date	.4/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P12	Serial No
Test Engineer	.Xen	
Date	.4/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.60	2.9µV√Hz	$\checkmark$
2		1.39	2.9µV√Hz	$\checkmark$
3		1.82	2.9µV√Hz	$\checkmark$
4		0.80	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P12	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P12.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P12	Serial No
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### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	$\checkmark$
Ch2	14mV	700uA	>2.5mA peak	$\checkmark$
Ch3	14mV	700uA	>2.5mA peak	$\checkmark$
Ch4	14mV	700uA	>2.5mA peak	$\checkmark$

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

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Date5/8	8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch2	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch3	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch4	1.68	2.4	118.8mA	>125mA peak	$\checkmark$

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Date	.5/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-90.8	-150.8	28.8	$\checkmark$
Ch2	-143.5	-91.0	-151.0	28.2	$\checkmark$
Ch3	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch4	-143.5	-92.6	-152.6	23.4	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ12....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ12P
Driver board ID	TACQ12
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON146
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

Drive Card ID.....T\_ACQ13..... Monitor Card ID...Mon186.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen..... Date.......6/8/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen..... Date.......3/8/10.....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen..... Date......3/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P13	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P13	Serial No
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### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	
2	1.93	5	1.86v r.m.s	
3	1.92	8	1.86v r.m.s	
4	1.92	11	1.86v r.m.s	

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.97	1	1.86v dc	The output is slightly high
2	1.97	4	1.86v dc	due to the output of the
3	1.97	7	1.86v dc	than calculated.
4	1.96	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.36	2.9µV√Hz	$\checkmark$
2		1.38	2.9µV√Hz	$\checkmark$
3		1.11	2.9µV√Hz	$\checkmark$
4		1.49	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P13	Serial No
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### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P13.....Serial No..... Test Engineer....Xen..... Date......3/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P13	Serial No
Test Engineer	Xen	
Date	.3/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo Specificatio (Vo/20) x 1.414		Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.237	16.8mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.243	17.2mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P13	Serial No
Test EngineerXe	n	
Date3/8	3/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	2.00	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch2	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch3	1.70	2.4	120.2mA	>125mA peak	$\checkmark$
Ch4	1.67	2.4	118.1mA	>125mA peak	$\checkmark$

Unit	.T_ACQ_P13	Serial No
Test Engineer	Xen	
Date	.3/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch2	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch3	-143.5	-91.0	-151.0	28.2	$\checkmark$
Ch4	-143.5	-93.5	-153.5	21.1	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ13.....Serial No ..... Test Engineer ......RMC Date .....2/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ13P
Driver board ID	TACQ13
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON186
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect. None
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen.... Date......6/8/10....

Drive Card ID.....T\_ACQ14..... Monitor Card ID...Mon187.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

## **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen..... Date.......6/8/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P14	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P14	Serial No
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Date	.3/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.97	1	1.86v dc	The output is slightly
2	1.97	4	1.86v dc	high due to the output of the driver being 1.2% higher than calculated
3	1.97	7	1.86v dc	
4	1.97	10	1.86v dc	

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give  $2.9\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.04	2.9µV√Hz	$\checkmark$
2		1.03	2.9µV√Hz	$\checkmark$
3		1.21	2.9µV√Hz	$\checkmark$
4		1.56	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P14	Serial No
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Date	.4/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P14.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P14	Serial No
Test Engineer	.Xen	
Date	4/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	12mV	600uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch3	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P14	Serial No
Test EngineerXe	en	
Date4/8	8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.66	2.3	117.4mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P14	Serial No
Test Engineer	Xen	
Date	.4/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch2	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch3	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch4	-143.5	-93.2	-153.2	21.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ14P.....Serial No ..... Test Engineer ......RMC Date ......1/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ14P
Driver board ID	TACQ14P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON187
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

Drive Card ID.....T\_ACQ15..... Monitor Card ID....Mon155.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
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- 8.2 Coil Monitors
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- 10.1 Noisy Mode
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- **10.3 Acquisition Mode**
- 11 Noise Measurements
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# **1. Description**

## **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen..... Date.......6/8/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P15	Serial No	
Test Engineer	Xen	-		
Date	.4/8/10			

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P15	Serial No
Test Engineer	Xen	
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### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.47	2.9µV√Hz	$\checkmark$
2		0.92	2.9µV√Hz	$\checkmark$
3		1.37	2.9µV√Hz	$\checkmark$
4		1.31	2.9µV√Hz	$\checkmark$

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Test Engineer	Xen	
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### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P15.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.417	29.5mA	>2.5mA peak	$\checkmark$
Ch2	0.417	29.5mA	>2.5mA peak	$\checkmark$
Ch3	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch4	0.416	29.4mA	>2.5mA peak	$\checkmark$
Unit	T ACQ P15	Serial No		
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Test Engineer	Xen			
Date	4/8/10			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.125	8.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P15	Serial No
Test Engineer>	en	
Date4	/8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch2	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch3	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch4	1.67	2.4	118.1mA	>125mA peak	$\checkmark$

Unit	.T_ACQ_P15	.Serial No
Test Engineer	.Xen	
Date	.4/8/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch2	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch3	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch4	-143.5	-92.3	-152.3	24.3	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ15P....Serial No ..... Test Engineer ......RMC Date .....1/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ15P
Driver board ID	TACQ15
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON155
Monitor board Drawing No/Issue No	D070480_4_K

#### 9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

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This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

Drive Card ID.....T\_ACQ16..... Monitor Card ID....Mon159....

# Contents

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# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P	16	.Serial No
Test Engineer	.Xen		
Date	.4/8/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P16	Serial No
Test Engineer	.Xen	
Date	.4/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.30	2.9µV√Hz	$\checkmark$
2		1.24	2.9µV√Hz	$\checkmark$
3		0.92	2.9µV√Hz	$\checkmark$
4		1.45	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P16	Serial No
Test Engineer	.Xen	
Date	.4/8/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P16.....Serial No..... Test Engineer....Xen..... Date......4/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.065	4.6mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.320	22.6mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P16	Serial No
Test Engineer	.Xen	
Date	.4/8/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P16	Serial No
Test EngineerX	en	
Date4/	/8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P16	Serial No
Test Engineer	.Xen	
Date	.4/8/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch2	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch3	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ16P.....Serial No ..... Test Engineer ......RMC Date ......1/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ16P
Driver board ID	TACQ16P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON159
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{\sqrt{}}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P17.....Serial No..... Test Engineer....Xen.... Date......15/9/10.....

Drive Card ID.....T\_ACQ17..... Monitor Card ID....Mon245....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P17.....Serial No..... Test Engineer....Xen.... Date......15/9/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	T ACQ	P17	Serial No
Test Engineer	.Xen		
Date	.14/9/10.		

# 3. Inspection

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P17	Serial No	
Test Engineer	.Xen	-		
Data	4 4 10 14 0			

Date.....14/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P17.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P17	Serial No
Test Engineer	Xen	
Date	.14/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P17	Serial No
Test Engineer	.Xen	
Date	.14/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.81	2.9µV√Hz	$\checkmark$
2		1.80	2.9µV√Hz	$\checkmark$
3		1.43	2.9µV√Hz	$\checkmark$
4		1.63	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P17	Serial No
Test Engineer	Xen	
Date	.15/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P17.....Serial No..... Test Engineer....Xen.... Date......15/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.328	23.2mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P17	Serial No
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## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P17	Serial No
Test Engineer	.Xen	
Date	.15/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T_ACQ	P17	Serial No
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Date	15/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch2	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch3	-143.5	-93.7	-153.7	20.7	$\checkmark$
Ch4	-143.5	-91.9	-151.9	25.4	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ17P.....Serial No ..... Test Engineer ......RMC Date ......1/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ17P
Driver board ID	TACQ17
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON245
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P18.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

Drive Card ID.....T\_ACQ18..... Monitor Card ID....Mon246....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P18.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P18.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P18	Serial No	
Test Engineer	.Xen	-		
Data	4 4 10 14 0			

Date.....14/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P18.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

#### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P18	Serial No
Test Engineer	Xen	
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P18	Serial No
Test Engineer	.Xen	
Date	.14/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.80	2.9µV√Hz	$\checkmark$
2		1.72	2.9µV√Hz	$\checkmark$
3		1.78	2.9µV√Hz	$\checkmark$
4		1.74	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P18	Serial No
Test Engineer	Xen	
Date	.14/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P18.....Serial No..... Test Engineer....Xen..... Date......14/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P18	Serial No
Test Engineer	Xen	
Date1	14/9/10	

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.134	9.5mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.134	9.5mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.251	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.251	17.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P18	Serial No
Test Engineer	Xen	
Date	14/9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.66	2.3	117.4mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ_P18	Serial No
Test Engineer	Xen	
Date	.14/9/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch3	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch4	-143.5	-92.7	-152.7	23.2	

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ18P.....Serial No ..... Test Engineer ......RMC Date ......1/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ18P
Driver board ID	TACQ18
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON246
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ19..... Monitor Card ID....Mon248.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P19.....Serial No..... Test Engineer....Xen.... Date......16/9/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P19.....Serial No..... Test Engineer....Xen.... Date......16/9/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P19Serial No
Test Engineer	.Xen	
Data	40/0/40	

Date.....16/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P19.....Serial No..... Test Engineer....Xen.... Date......16/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

#### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P19	Serial No
Test Engineer	.Xen	
Date	.16/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P19	Serial No
Test Engineer	.Xen	
Date	.16/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

#### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.47	2.9µV√Hz	$\checkmark$
2		1.68	2.9µV√Hz	$\checkmark$
3		1.55	2.9µV√Hz	$\checkmark$
4		1.56	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P19	.Serial No
Test Engineer	.Xen	
Date	.16/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P19.....Serial No..... Test Engineer....Xen..... Date......16/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P19	Serial No
Test Engineer	Xen	
Date	16/9/10	

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	13mV	650uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch2	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch3	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P19	Serial No
Test Engineer	Xen	
Date1	16/9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T_ACQ_F	P19	Serial No
Test Engineer	.Xen		
Date	16/9/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch2	-143.5	-91.1	-151.1	27.9	$\checkmark$
Ch3	-143.5	-92.6	-152.6	23.4	$\checkmark$
Ch4	-143.5	-93.2	-153.2	21.9	

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ19P.....Serial No ..... Test Engineer ......RMC Date .....

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ19P
Driver board ID	TACQ19
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON248
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ20..... Monitor Card ID....Mon247.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
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# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P20....Serial No.... Test Engineer....Xen.... Date......16/9/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P20.....Serial No..... Test Engineer....Xen..... Date......15/9/10.....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P20Serial No	
Test Engineer	.Xen		
Data	4 = 10 14 0		

Date.....15/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P20.....Serial No..... Test Engineer....Xen..... Date......15/9/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P20	Serial No
Test Engineer	.Xen	
Date	.15/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P20	Serial No
Test Engineer	.Xen	
Date	.15/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9µV√Hz	$\checkmark$
2		1.40	2.9µV√Hz	$\checkmark$
3		1.68	2.9µV√Hz	$\checkmark$
4		1.44	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P20	.Serial No
Test Engineer	.Xen		
Date	.15/9/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P20.....Serial No..... Test Engineer....Xen.... Date......15/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P20	.Serial No
Test Engineer	Xen	-	
Date	16/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ I	P20	Serial No
Test Engineer	.Xen		
Date	16/9/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ P	20	.Serial No
Test Engineer	.Xen		
Date	15/9/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-90.2	-150.2	30.9	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ20P.....Serial No ..... Test Engineer ......RMC Date .....13/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ20P
Driver board ID	TACQ20
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON247
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P21.....Serial No..... Test Engineer....Xen.... Date......13/9/10.....

Drive Card ID.....T\_ACQ21..... Monitor Card ID....Mon237.....

## Contents

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- **10.3 Acquisition Mode**
- 11 Noise Measurements
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## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P21.....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	T ACQ	P21	Serial No
Test Engineer	.Xen	-	
Date	13/9/10		

## 3. Inspection

## Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P21	Serial No	
Test Engineer	.Xen	-		
Data	4010140			

Date.....13/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P21.....Serial No..... Test Engineer....Xen..... Date......13/9/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P21	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P21	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.50	2.9µV√Hz	$\checkmark$
2		1.65	2.9µV√Hz	$\checkmark$
3		1.74	2.9µV√Hz	$\checkmark$
4		1.49	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P21	Serial No
Test Engineer	Xen	
Date	.13/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P21.....Serial No..... Test Engineer....Xen.... Date......13/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P21	.Serial No
Test Engineer	.Xen	-	
Date	13/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P21	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.1	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T ACQ P21	.Serial No
Test Engineer	.Xen	
Date	.13/9/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.8	-153.8	20.4	$\checkmark$
Ch2	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch3	-143.5	-93.6	-153.6	20.9	$\checkmark$
Ch4	-143.5	-94.0	-154.0	20.0	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ21P....Serial No ..... Test Engineer ......RMC Date .....13/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ21P
Driver board ID	TACQ21P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON237
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P22.....Serial No..... Test Engineer....Xen.... Date......13/9/10.....

Drive Card ID.....T\_ACQ22.... Monitor Card ID....Mon238....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
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- **10.3 Acquisition Mode**
- 11 Noise Measurements
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## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P22....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P22....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_	_P22	Serial No
Test Engineer	.Xen		

Date.....13/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P22....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P22	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P22	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.66	2.9µV√Hz	$\checkmark$
2		1.59	2.9µV√Hz	$\checkmark$
3		1.60	2.9µV√Hz	$\checkmark$
4		1.84	2.9µV√Hz	$\checkmark$

Unit	T ACQ I	P22	Serial No
Test Engineer	.Xen		
Date	.13/9/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P22....Serial No..... Test Engineer....Xen.... Date......13/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P22	Serial No
Test Engineer	Xen	
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## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	13mV	650uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	12mV	600uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P	22Serial No
Test EngineerXe	en	
Date13	/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.1	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ F	P22	Serial No
Test Engineer	.Xen		
Date	.13/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.1	-151.1	27.9	$\checkmark$
Ch2	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch3	-143.5	-84.7	-144.7	58.2	$\checkmark$
Ch4	-143.5	-91.6	-151.6	26.3	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ22P....Serial No ..... Test Engineer ......RMC Date .....13/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ22P
Driver board ID	TACQ22
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON238
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

Drive Card ID.....T\_ACQ23..... Monitor Card ID....Mon259....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen....

Date......24/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P23	Serial No
Test Engineer	Xen	
Date	.24/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P23	Serial No
Test Engineer	.Xen	
Date	.24/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.69	2.9µV√Hz	$\checkmark$
2		1.86	2.9µV√Hz	$\checkmark$
3		1.44	2.9µV√Hz	$\checkmark$
4		1.42	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P23	Serial No
Test Engineer	.Xen		
Date	.24/9/10.		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P23.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P23	Serial No
Test Engineer	.Xen	
Date	24/9/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.134	9.5mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.252	17.8mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P2	3Serial No
Test EngineerXe	- — en	
Date24	/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T ACQ	P23	Serial No
Test Engineer	.Xen	-	
Date	24/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch3	-143.5	-92.9	-152.9	22.9	$\checkmark$
Ch4	-143.5	-93.5	-153.5	21.1	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ23P....Serial No ..... Test Engineer ......RMC Date .....13/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ23P
Driver board ID	TACQ23
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON259
Monitor board Drawing No/Issue No	D070480 5 K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P24.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

Drive Card ID.....T\_ACQ24..... Monitor Card ID....Mon260.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P24.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P24.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P24	Serial No	
Test Engineer		-		
Data	04/0/40			

Date.....24/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P24.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P24	Serial No
Test Engineer	.Xen	
Date	.24/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P24	Serial No
Test Engineer	.Xen	
Date	.24/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.90	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.82	2.9µV√Hz	$\checkmark$
2		1.77	2.9µV√Hz	$\checkmark$
3		1.63	2.9µV√Hz	$\checkmark$
4		1.51	2.9µV√Hz	$\checkmark$

Unit	T ACQ P24	Serial No
Test Engineer	.Xen	
Date	24/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P24.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
Unit	F ACQ F	24Serial	No	
----------------	---------	----------	----	
Test Engineer>	Ken			
Date2	24/9/10			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.124	8.8mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.239	16.9mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.250	17.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P2	4Serial No
Test Engineer	Xen	
Date	24/9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T ACQ P24	Serial No
Test Engineer	Xen	
Date	.24/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch2	-143.5	-93.6	-153.6	20.9	$\checkmark$
Ch3	-143.5	-94.3	-154.3	19.3	$\checkmark$
Ch4	-143.5	-93.4	-153.4	21.4	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ24P....Serial No ..... Test Engineer ......RMC Date .....13/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ24P
Driver board ID	TACQ24
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON260
Monitor board Drawing No/Issue No	D070480 5 K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

Drive Card ID.....T\_ACQ25..... Monitor Card ID....Mon150.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen

Date......25/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P25	.Serial No
Test Engineer	.Xen	-	
Date	25/8/10.		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ F	P25	Serial No
Test Engineer	.Xen		
Date	25/8/10		

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.55	2.9µV√Hz	$\checkmark$
2		1.39	2.9µV√Hz	$\checkmark$
3		1.01	2.9µV√Hz	$\checkmark$
4		1.41	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P25	Serial No
Test Engineer	Xen		
Date	.25/8/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P25.....Serial No..... Test Engineer....Xen.... Date......25/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

UnitT	<sup>-</sup> ACQ P25	Serial No
Test Engineer	en	
Date2	5/8/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	13.5mV	675uA	>2.5mA peak	
Ch3	13.5mV	675uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch3	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch3	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P25	.Serial No
Test Engineer	Xen	-	
Date	25/8/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T ACQ	P25	Serial No
Test Engineer	Xen	-	
Date	.25/8/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch2	-143.5	-94.3	-154.3	19.3	$\checkmark$
Ch3	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch4	-143.5	-91.9	-151.9	25.4	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ25P....Serial No ..... Test Engineer ......RMC Date .....14/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ25P
Driver board ID	TACQ25P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON150
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P26.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

Drive Card ID.....T\_ACQ26..... Monitor Card ID....Mon151.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
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- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P26.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P26.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_	P26	Serial No	
Test Engineer	.Xen	- 		
Data	05/0/40			

Date.....25/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P26.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P26	.Serial No
Test Engineer	.Xen	-	
Date	25/8/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P26	Serial No
Test Engineer	.Xen	
Date	.25/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.47	2.9µV√Hz	$\checkmark$
2		1.37	2.9µV√Hz	$\checkmark$
3		0.96	2.9µV√Hz	$\checkmark$
4		1.88	2.9µV√Hz	$\checkmark$

Unit	T ACQ P26	.Serial No
Test Engineer	Xen	
Date	.25/8/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P26.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P26	.Serial No
Test Engineer	Xen		
Date	25/8/10		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

_	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	9.3mA >2.5mA peak	
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P2	3Serial No
Test EngineerXe	n	
Date25/	8/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch2	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch3	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch4	1.66	2.3	117.4mA	>125mA peak	$\checkmark$

Unit	T ACQ	P26	.Serial No
Test Engineer	Xen	-	
Date	.25/8/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-91.1	-151.1	27.9	$\checkmark$
Ch3	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch4	-143.5	-93.1	-153.1	22.1	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ26P....Serial No ..... Test Engineer ......RMC Date .....14/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ26P
Driver board ID	TACQ26
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON151
Monitor board Drawing No/Issue No	D070480/4/K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P27.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

Drive Card ID......T\_ACQ27..... Monitor Card ID....Mon144....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P27....Serial No.... Test Engineer....Xen.... Date......6/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P27.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P27.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P27.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P27	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P27	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.05	2.9µV√Hz	$\checkmark$
2		0.99	2.9µV√Hz	$\checkmark$
3		1.14	2.9µV√Hz	$\checkmark$
4		1.51	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P27	Serial No
Test Engineer	Xen	
Date	.5/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P27.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P27	Serial No
Test Engineer	.Xen	-	
Date	.5/8/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P27	Serial No
Test EngineerXe	en	
Date5/8	3/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P27	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch2	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ27P.....Serial No ..... Test Engineer ......RMC Date .....14/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ27P
Driver board ID	TACQ27
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON144
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P28.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

Drive Card ID.....T\_ACQ28.... Monitor Card ID...Mon216....

### **Contents**

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P28.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P28.....Serial No..... Test Engineer....Xen..... Date......7/10/10.....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P28	Serial No	
Test Engineer	Xen	-		
Data	7/10/10			

Date.....7/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P28.....Serial No..... Test Engineer....Xen..... Date......7/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P28	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P28	Serial No
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Date	.7/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.45	2.9µV√Hz	$\checkmark$
2		1.55	2.9µV√Hz	$\checkmark$
3		1.38	2.9µV√Hz	$\checkmark$
4		1.53	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P28	Serial No
Test Engineer	.Xen		
Date	.8/10/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P28.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P28	.Serial No
Test Engineer	.Xen	-	
Date	.8/10/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.131	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit1		P28	.Serial No
Test Engineer>	(en	-	
Date8	/10/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T_ACQ_P28	Serial No
Test Engineer	.Xen	
Date	7/10/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch2	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-91.8	-151.8	25.7	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ29P....Serial No ..... Test Engineer ......RMC Date ......4/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ29P
Driver board ID	TACQ29P
Driver board Drawing No/Issue No	D0901047v4
Monitor board ID	MON244
Monitor board Drawing No/Issue No	DO7O480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P29.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

Drive Card ID.....T\_ACQ29..... Monitor Card ID...Mon244....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P29....Serial No.... Test Engineer....Xen.... Date......14/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P29....Serial No.... Test Engineer....Xen.... Date......14/9/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P29	Serial No	
Test Engineer		-		
Data	4 4 10 14 0			

Date.....14/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P29.....Serial No..... Test Engineer....Xen..... Date......14/9/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P29	Serial No
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## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P29	Serial No
Test Engineer	.Xen	
Date	.14/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9µV√Hz	$\checkmark$
2		1.46	2.9µV√Hz	$\checkmark$
3		1.78	2.9µV√Hz	$\checkmark$
4		1.65	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P29	Serial No
Test Engineer	.Xen		
Date	.14/9/10.		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P29.....Serial No..... Test Engineer....Xen.... Date......14/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.412	29.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P29	Serial No
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Date	14/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.243	17.2mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_	P29	.Serial No
Test Engineer	Xen	-	
Date	14/9/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.66	2.4	117.4mA	>125mA peak	
Ch4	1.65	2.3	116.7mA	>125mA peak	

Unit	T ACQ	P29	.Serial No
Test Engineer	.Xen	-	
Date	.14/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-91.2	-151.2	27.5	$\checkmark$
Ch4	-143.5	-92.7	-152.7	23.2	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ28P....Serial No ..... Test Engineer ......RMC Date .....14/10//10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ28P
Driver board ID	TACQ28
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON216
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ30..... Monitor Card ID...Mon241.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P30.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P30.....Serial No..... Test Engineer....Xen.... Date......13/9/10.....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P30	Serial No	
Test Engineer	.Xen	-		
Data	40/0/40			

Date.....13/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P30.....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P30	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P30	Serial No
Test Engineer	.Xen	
Date	.13/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9µV√Hz	$\checkmark$
2		1.39	2.9µV√Hz	$\checkmark$
3		1.55	2.9µV√Hz	$\checkmark$
4		1.69	2.9µV√Hz	$\checkmark$

Unit	T ACQ P30	)Serial No
Test Engineer	.Xen	
Date	14/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P30.....Serial No..... Test Engineer....Xen.... Date......14/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P30	.Serial No
Test Engineer	.Xen	-	
Date	14/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P30	Serial No
Test Engineer	Xen	
Date	14/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ P	30	Serial No
Test Engineer	.Xen		
Date	14/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-86.4	-146.4	47.9	$\checkmark$
Ch2	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch3	-143.5	-93.9	-153.9	20.2	$\checkmark$
Ch4	-143.5	-92.8	-152.8	22.9	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ30P.....Serial No ..... Test Engineer ......RMC Date ......18/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ30P
Driver board ID	TACQ30
Driver board Drawing No/Issue No	D090147_V4
Monitor board ID	MON241
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

Drive Card ID.....T\_ACQ31..... Monitor Card ID....Mon172.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
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- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL			To J1 PIN	OK?
1	Imon1P				$\checkmark$
2	Imon2P			6	$\checkmark$
3	Imon3P			7	$\checkmark$
4	Imon4P	8		$\checkmark$	
	5	0V		$\checkmark$	
6	Imon1N			18	$\checkmark$
7	Imon2N			19	$\checkmark$
8	Imon3N			20	$\checkmark$
9	Imon4N			21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P31	.Serial No
Test Engineer	Xen	
Date	.5/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P31	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.11	2.9µV√Hz	$\checkmark$
2		1.07	2.9µV√Hz	$\checkmark$
3		1.24	2.9µV√Hz	$\checkmark$
4		1.10	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P31	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P31.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P31	Serial No
Test Engineer	Xen	
Date	.5/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.121	8.6mA	>2.5mA peak	$\checkmark$
Ch3	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.235	16.6mA	>2.5mA peak	$\checkmark$
Ch3	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch3	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P31	Serial No
Test EngineerXe	èn	
Date5/8	3/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch2	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch3	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch4	1.67	2.4	118.1mA	>125mA peak	$\checkmark$

Unit	.T_ACQ_P31	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch3	-143.5	-93.2	-153.2	21.9	$\checkmark$
Ch4	-143.5	-91.3	-151.3	27.2	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ31P.....Serial No ..... Test Engineer ......RMC Date ......18/10/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ31P
Driver board ID	TACQ31
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON172
Monitor board Drawing No/Issue No	D070480_04_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

Drive Card ID.....T\_ACQ32..... Monitor Card ID....Mon173.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

## **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen..... Date......5/8/10.....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P32	Serial No
Test Engineer	.Xen	
Date	.5/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P32	Serial No
Test Engineer	Xen	
Date6	5/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.35	2.9µV√Hz	$\checkmark$
2		1.99	2.9µV√Hz	$\checkmark$
3		1.30	2.9µV√Hz	$\checkmark$
4		1.06	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P32	Serial No
Test Engineer	Xen	
Date	.6/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P32.....Serial No..... Test Engineer....Xen..... Date......6/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P32	Serial No
Test Engineer	.Xen	
Date	.6/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750mA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P32	Serial No
Test EngineerXe	n	
Date6/8	3/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

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### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.9	-151.9	25.4	$\checkmark$
Ch2	-143.5	-93.2	-153.2	21.9	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-93.2	-153.2	21.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ32P....Serial No ..... Test Engineer ......RMC Date ......18/10/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ32P
Driver board ID	TACQ32
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON173
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P33.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

Drive Card ID.....T\_ACQ33..... Monitor Card ID...Mon227....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

## **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P33.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P33.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P33	Serial No	
Test Engineer	Xen	_ 		
Data	10/0/10			

Date.....19/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P33.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P33	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P33	Serial No
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### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.57	2.9µV√Hz	$\checkmark$
2		1.68	2.9µV√Hz	$\checkmark$
3		1.56	2.9µV√Hz	$\checkmark$
4		1.39	2.9µV√Hz	$\checkmark$

Unit	T ACQ P33.	Serial No
Test Engineer	.Xen	
Date	19/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P33.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.065	4.6mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$
Unit	T ACQ P33	Serial No		
---------------	-----------	-----------		
Test Engineer	.Xen			
Date	19/8/10			

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch3	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.125	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch2	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch3	0.240	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P33	Serial No
Test Engineer	Xen	
Date	19/8/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T ACQ	P33	.Serial No
Test Engineer	.Xen	-	
Date	19/8/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch2	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch3	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch4	-143.5	-92.7	-152.7	23.2	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ33P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ33P
Driver board ID	TACQ33
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON227
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P34.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

Drive Card ID.....T\_ACQ34..... Monitor Card ID...Mon226....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P34.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P34.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P34	.Serial No
Test Engineer			
Data	40/0/40		

Date.....19/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P34.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P34	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P34	Serial No
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# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.60	2.9µV√Hz	$\checkmark$
2		1.94	2.9µV√Hz	$\checkmark$
3		1.79	2.9µV√Hz	$\checkmark$
4		1.62	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P34	Serial No
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Date	.19/8/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P34.....Serial No..... Test Engineer....Xen.... Date......19/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P34	Serial No
Test Engineer	.Xen	-	
Date	19/8/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Peak lo Specification (Vo/20) x 1.414	
Ch1	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch2	0.122	8.6mA	>2.5mA peak	$\checkmark$
Ch3	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch2	0.237	16.8mA	>2.5mA peak	$\checkmark$
Ch3	0.233	16.5mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P34	Serial No
Test Engineer	Xen	
Date	19/8/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	2.00	2.8	141.4mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T ACQ P34	Serial No
Test Engineer	.Xen	
Date	.19/8/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch3	-143.5	-89.3	-149.3	34.3	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ34P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ34P
Driver board ID	TACQ34
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON226
Monitor board Drawing No/Issue No	D070480_05_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P35.....Serial No..... Test Engineer....Xen.... Date......18/7/10.....

Drive Card ID......T\_ACQ35..... Monitor Card ID......Mon225.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P35.....Serial No..... Test Engineer....Xen.... Date......18/7/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P35.....Serial No..... Test Engineer....Xen.... Date......18/7/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P35	Serial No	
Test Engineer	Xen			
Data	10/7/10			

Date.....18/7/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL			To J1 PIN	OK?
1	Imon1P			5	$\checkmark$
2	Imon2P			6	$\checkmark$
3	Imon3P			7	$\checkmark$
4	Imon4P			8	$\checkmark$
	5	0V		$\checkmark$	
6	Imon1N			18	$\checkmark$
7	Imon2N			19	$\checkmark$
8	Imon3N			20	$\checkmark$
9	Imon4N			21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P35.....Serial No..... Test Engineer....Xen.... Date......18/7/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P35	.Serial No
Test Engineer	.Xen	-	
Date	18/7/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P35	Serial No
Test Engineer	.Xen	
Date	.18/7/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.62	2.9µV√Hz	$\checkmark$
2		1.91	2.9µV√Hz	$\checkmark$
3		1.60	2.9µV√Hz	$\checkmark$
4		1.59	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P35	Serial No
Test Engineer	.Xen		
Date	.18/7/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P35.....Serial No..... Test Engineer....Xen..... Date......18/7/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	65mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P35	.Serial No
Test Engineer	.Xen	-	
Date	18/7/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.122	8.6mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.236	16.7mA	>2.5mA peak	$\checkmark$
Ch2	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P35	.Serial No
Test Engineer	.Xen	-	
Date	18/7/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ	P35	Serial No
Test Engineer	Xen	-	
Date	.18/7/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-94.0	-154.0	20.0	$\checkmark$
Ch2	-143.5	-93.2	-153.2	21.9	$\checkmark$
Ch3	-143.5	-91.0	-151.0	28.2	$\checkmark$
Ch4	-143.5	-92.8	-152.8	22.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ35P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ35P
Driver board ID	TACQ35
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON225
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ36..... Monitor Card ID....Mon223....

## Contents

- 1 Description
- 2 Test Equipment
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- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P36.....Serial No..... Test Engineer....Xen..... Date......18/8/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P36.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P36	Serial No	
Test Engineer	.Xen	•		
D-4-	4710140			

Date.....17/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P36.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P36	.Serial No
Test Engineer	.Xen	-	
Date	17/8/10.		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P36	Serial No
Test Engineer	.Xen	
Date	.17/8/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.62	2.9µV√Hz	$\checkmark$
2		1.32	2.9µV√Hz	$\checkmark$
3		1.25	2.9µV√Hz	$\checkmark$
4		1.44	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P36	Serial No
Test Engineer	.Xen		
Date	.18/8/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P36.....Serial No..... Test Engineer....Xen.... Date......18/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P36	.Serial No
Test Engineer	.Xen	-	
Date	18/8/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.131	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.248	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P36	Serial No
Test Engineer	Xen	••••••	
Date1	18/8/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	2.00	2.8	141.4mA	>125mA peak	$\checkmark$
Ch4	2.00	2.8	141.4mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch2	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch3	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch4	1.68	2.4	118.8mA	>125mA peak	$\checkmark$

Unit	.T_ACQ	P36	Serial No
Test Engineer	Xen	-	
Date	.17/8/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-90.3	-150.3	30.5	$\checkmark$
Ch2	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-93.1	-153.1	22.1	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ36P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ36P
Driver board ID	TACQ36
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON223
Monitor board Drawing No/Issue No	D070480_05_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ37..... Monitor Card ID...Mon224.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P37.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P37.....Serial No..... Test Engineer....Xen..... Date......17/8/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P37	Serial No	
Test Engineer	.Xen	-		
Data	47/0/40			

Date.....17/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P37.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P37	Serial No
Test Engineer	Xen	
Date	17/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P37	Serial No
Test Engineer	.Xen	
Date	.17/8/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.64	2.9µV√Hz	$\checkmark$
2		1.47	2.9µV√Hz	$\checkmark$
3		1.82	2.9µV√Hz	$\checkmark$
4		1.77	2.9µV√Hz	$\checkmark$

Unit	T ACQ P37	Serial No
Test Engineer	.Xen	
Date	17/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P37.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P37	Serial No
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### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	_ACQ_P37	Serial No
Test EngineerX	en	
Date17	7/8/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

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Test Engineer	.Xen	-		
Date	.17/8/10.			

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch4	-143.5	-91.0	-151.0	28.1	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ37P.....Serial No ..... Test Engineer ......RMC Date ......21/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ37P
Driver board ID	TACQ37
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON224
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ38..... Monitor Card ID...Mon221.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P38.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P38.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

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Date.....16/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P38.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P38	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P38	Serial No
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## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.90	5	1.86v r.m.s	$\checkmark$
3	1.90	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		2.02	2.9µV√Hz	$\checkmark$
2		1.80	2.9µV√Hz	$\checkmark$
3		1.52	2.9µV√Hz	$\checkmark$
4		1.81	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P38	Serial No
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Date	.17/8/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P38.....Serial No..... Test Engineer....Xen.... Date......17/8/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P38	.Serial No
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Date	17/8/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch2	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.122	8.6mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch2	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.236	16.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P38	.Serial No
Test Engineer	Xen	
Date	17/8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P38	.Serial No
Test Engineer	.Xen	-	
Date	16/8/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch2	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch3	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ38P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ38P
Driver board ID	TACQ38
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON221
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ39..... Monitor Card ID....Mon175.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P39.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P39.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P39	Serial No	
Test Engineer		-		
Data	0/40/40			

Date......8/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P39.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P39	Serial No
Test Engineer	.Xen	
Date	.8/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P39	Serial No
Test Engineer	.Xen	
Date	.8/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.45	2.9µV√Hz	$\checkmark$
2		1.39	2.9µV√Hz	$\checkmark$
3		1.50	2.9µV√Hz	$\checkmark$
4		1.42	2.9µV√Hz	$\checkmark$

Unit	T ACQ F	<b>&gt;</b> 39	.Serial No
Test Engineer	.Xen		
Date	.8/10/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P39.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P39	Serial No
Test Engineer	.Xen	-	
Date	8/10/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_	P39	.Serial No
Test Engineer	.Xen	-	
Date	8/10/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P39	.Serial No
Test Engineer	.Xen		
Date	8/10/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-89.7	-149.7	32.7	$\checkmark$
Ch3	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ39P.....Serial No ..... Test Engineer ......RMC Date ......19/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ39P
Driver board ID	TACQ39
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON175
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ40..... Monitor Card ID....Mon156....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P40.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	<sup>2</sup> 40Serial No
Test Engineer	.Xen	
D-4-	0/40/40	

Date......8/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P40.....Serial No..... Test Engineer....Xen.... Date......8/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P40	Serial No	
Test Engineer	.Xen		
Date	.8/10/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P40	Serial No
Test Engineer	.Xen	
Date	.8/10/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.18	2.9µV√Hz	$\checkmark$
2		1.43	2.9µV√Hz	$\checkmark$
3		1.36	2.9µV√Hz	$\checkmark$
4		1.55	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P40	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P4	40Serial No
Test EngineerX	en	
Date11	/10/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	47mV	2.3mA	>2.5mA peak	
Ch2	47mV	2.3mA	>2.5mA peak	
Ch3	47mV	2.3mA	>2.5mA peak	
Ch4	47mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.240	17.0mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P40	Serial No
Test EngineerXe	en	
Date11	/10/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T_ACQ_	P40	Serial No
Test Engineer	.Xen		
Date	8/10/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch3	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch4	-143.5	-91.6	-151.6	26.3	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ40P.....Serial No ..... Test Engineer ......RMC Date ......21/10/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ40P
Driver board ID	TACQ40
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON156
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P41.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

Drive Card ID.....T\_ACQ41..... Monitor Card ID....Mon255.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
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- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P41.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P41.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P41	Serial No	
Test Engineer	Xen	-		
Data	00/0/40			

Date.....22/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P41.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P41	Serial No
Test Engineer	Xen	
Date	.22/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P41	Serial No
Test Engineer	.Xen	
Date	.22/9/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	2	1.86v r.m.s	$\checkmark$
2	1.94	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.98	1	1.86v dc	
2	1.98	4	1.86v dc	
3	1.97	7	1.86v dc	
4	1.97	10	1.86v dc	

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.42	2.9µV√Hz	$\checkmark$
2		1.88	2.9µV√Hz	$\checkmark$
3		1.53	2.9µV√Hz	$\checkmark$
4		1.63	2.9µV√Hz	$\checkmark$

Unit	T ACQ P41	Serial No
Test Engineer	Xen	
Date	.23/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P41.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.413	29.2mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ I	P41	Serial No
Test Engineer	Xen		
Date	23/9/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	13mV	650uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P41	Serial No
Test EngineerXe	en	
Date23	/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	.T_ACQ_P41	Serial No	
Test Engineer	.Xen		
Date	.23/9/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch4	-143.5	-92.3	-152.3	24.3	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ41P.....Serial No ..... Test Engineer ......RMC Date ......21/10/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ41P
Driver board ID	TACQ41
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON255
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

Drive Card ID.....T\_ACQ42..... Monitor Card ID...Mon256.....

### **Contents**

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen....

Date......22/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P42	Serial No	
Test Engineer	.Xen		
Date	.22/9/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P42	Serial No
Test Engineer	.Xen	
Date	.22/9/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.72	2.9µV√Hz	$\checkmark$
2		2.04	2.9µV√Hz	$\checkmark$
3		1.29	2.9µV√Hz	$\checkmark$
4		1.33	2.9µV√Hz	$\checkmark$

Unit	T ACQ P42	Serial No
Test Engineer	.Xen	
Date	.22/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P42.....Serial No..... Test Engineer....Xen..... Date......22/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
Unit	T ACQ P42	Serial No		
---------------	-----------	-----------		
Test Engineer	Xen			
Date	22/9/10			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	12mV	600uA	>2.5mA peak	
Ch4	12mV	600uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P42.	Serial No
Test EngineerXe	en	
Date22	/9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P42	Serial No
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Date	.22/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch2	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-90.7	-150.7	29.2	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ42P....Serial No ..... Test Engineer ......RMC Date ......21/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ42P
Driver board ID	TACQ42
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON257
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P43.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

Drive Card ID.....T\_ACQ43..... Monitor Card ID....Mon252....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P43.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P43.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P43	Serial No
Test Engine	erXen	
<b>D</b> (	0.1.10.1.1.0	

Date.....21/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P43.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P43	.Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P43	Serial No
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Date	.21/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.65	2.9µV√Hz	$\checkmark$
2		1.35	2.9µV√Hz	$\checkmark$
3		1.71	2.9µV√Hz	$\checkmark$
4		1.56	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P43	.Serial No
Test Engineer	Xen	
Date	.21/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P43.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P43	Serial No
Test Engineer	Xen	
Date2	21/9/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specificat (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P43	Serial No
Test Engineer	Xen	
Date	21/9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T_ACQ_P43	Serial No
Test Engineer	.Xen	
Date	21/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch2	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch3	-143.5	-90.7	-150.7	29.2	$\checkmark$
Ch4	-143.5	-93.7	-153.7	20.7	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ43P....Serial No ..... Test Engineer ......RMC Date ......21/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ43P
Driver board ID	TACQ43P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON252
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P44.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

Drive Card ID.....T\_ACQ44..... Monitor Card ID....Mon251.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P44.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P44....Serial No..... Test Engineer....Xen.... Date......21/9/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T_ACQ	P44.	Serial No
Test Engineer	·Xen		

Date.....21/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P44.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P44	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P44	Serial No
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Date	.21/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.48	2.9µV√Hz	$\checkmark$
2		1.44	2.9µV√Hz	$\checkmark$
3		1.49	2.9µV√Hz	$\checkmark$
4		1.66	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P44	Serial No
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Date	.22/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P44.....Serial No..... Test Engineer....Xen.... Date......22/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P44	Serial No
Test EngineerXe	en	
Date22	2/9/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	13mV	650uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_	P44	.Serial No
Test Engineer	Xen	-	
Date	22/9/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P44	Serial No
Test Engineer	.Xen	
Date	21/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.6	-152.6	23.4	$\checkmark$
Ch2	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch3	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch4	-143.5	-93.6	-153.6	20.9	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ44P....Serial No ..... Test Engineer ......RMC Date ......21/10/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ44P
Driver board ID	TACQ44P
Driver board Drawing No/Issue No	D090047_V4
Monitor board ID	MON251
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P45.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

Drive Card ID.....T\_ACQ45..... Monitor Card ID....Mon254....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P45.....Serial No..... Test Engineer....Xen.... Date......21/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P45.....Serial No..... Test Engineer....Xen.... Date......20/9/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P45.....Serial No..... Test Engineer.....Xen

Date......20/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P45.....Serial No..... Test Engineer....Xen.... Date......20/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P45	Serial No
Test Engineer	.Xen	
Date	20/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P45	.Serial No
Test Engineer	.Xen	
Date	.21/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.97	2.9µV√Hz	$\checkmark$
2		1.82	2.9µV√Hz	$\checkmark$
3		1.65	2.9µV√Hz	$\checkmark$
4		1.84	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P45	Serial No
Test Engineer	.Xen	
Date	.21/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P45.....Serial No..... Test Engineer....Xen..... Date......21/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P45	.Serial No
Test Engineer	.Xen		
Date	.21/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	13mV	650uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch4	0.123	8.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch4	0.237	16.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_	P45	.Serial No
Test Engineer	Xen	-	
Date	21/9/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.1	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T_ACQ	P45	Serial No
Test Engineer	.Xen	-	
Date	21/9/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch2	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch3	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch4	-143.5	-91.3	-151.3	27.2	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ45P....Serial No ..... Test Engineer ......RMC Date ......21/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ45P
Driver board ID	TACQ45P
Driver board Drawing No/Issue No	D0902047_V4
Monitor board ID	MON254
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires.  $\sqrt{}$ 

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P46.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

Drive Card ID.....T\_ACQ46..... Monitor Card ID...Mon184.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
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- 8 Monitor Outputs
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- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P46.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P46.....Serial No..... Test Engineer....Xen.... Date......28/9/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P46	Serial No	
Test Engineer	.Xen	-		
Data	00/0/40			

Date......28/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+ 4		$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P46.....Serial No..... Test Engineer....Xen.... Date......28/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P46	.Serial No
Test Engineer	.Xen		
Date	.28/9/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P46	Serial No
Test Engineer	.Xen	
Date	.28/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.59	2.9µV√Hz	$\checkmark$
2		1.49	2.9µV√Hz	$\checkmark$
3		1.73	2.9µV√Hz	$\checkmark$
4		1.29	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P46	Serial No
Test Engineer	.Xen		
Date	.29/9/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P46.....Serial No..... Test Engineer....Xen..... Date......29/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.326	23.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.391	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P46	.Serial No
Test Engineer	Xen	• • • • • • • • • • • • • • • • • • • •	
Date	29/9/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P46	Serial No
Test EngineerXe	n	
Date29/	9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.4	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.4	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.4	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.4	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ	P46	.Serial No
Test Engineer	.Xen	-	
Date	.28/9/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch4	-143.5	-93.7	-153.7	20.7	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ46P....Serial No ..... Test Engineer ......RMC Date ......21/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ46P
Driver board ID	TACQ46P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON184
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P47.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

Drive Card ID.....T\_ACQ47..... Monitor Card ID....Mon262....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P47.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P47.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P47	Serial No
Test Engine	eer <mark>Xe</mark> n	

Date.....27/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P47.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P47	Serial No
Test Engineer	.Xen	
Date	.27/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P47	Serial No
Test Engineer	.Xen	
Date	.27/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.71	2.9µV√Hz	$\checkmark$
2		1.86	2.9µV√Hz	$\checkmark$
3		1.73	2.9µV√Hz	$\checkmark$
4		1.53	2.9µV√Hz	$\checkmark$

Unit	T ACQ P47	Serial No
Test Engineer	Xen	
Date	27/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P47.....Serial No..... Test Engineer....Xen.... Date......27/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.326	23.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.391	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P47	Serial No
Test Engineer	Xen	
Date	27/9/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	_ACQ_P47	Serial No
Test EngineerX	.en	
Date27	7/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.99	2.8	140.7mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P47	Serial No	
Test Engineer	.Xen	-		
Date	27/9/10			

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch2	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch3	-143.5	-93.2	-153.2	21.9	$\checkmark$
Ch4	-143.5	-92.2	-152.2	24.5	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ47P.....Serial No ..... Test Engineer ......RMC Date ......21/10/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight  $\sqrt{}.$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ47P
Driver board ID	TACQ47P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON262
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P48.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

Drive Card ID.....T\_ACQ48..... Monitor Card ID....Mon261.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P48.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P48.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P48	Serial No
Test Engineer	.Xen		
Data	04/0/40		

Date.....24/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
	5	0V	$\checkmark$	
6	PD1N	Photodiode A- 14		$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
	5	0V	$\checkmark$	
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P48.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P48	Serial No
Test Engineer	Xen	
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P48	Serial No
Test Engineer	.Xen	
Date	.24/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	$\checkmark$

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.61	2.9µV√Hz	$\checkmark$
2		1.55	2.9µV√Hz	$\checkmark$
3		1.66	2.9µV√Hz	$\checkmark$
4		1.54	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P48	Serial No
Test Engineer	Xen	
Date	.27/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P48.....Serial No..... Test Engineer....Xen.... Date......27/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.391	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.417	29.5mA	>2.5mA peak	$\checkmark$
Ch3	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	<sup>-</sup> ACQ P48	Serial No
Test Engineer>	en	
Date2	7/9/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	13mV	650uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	o r.m.s Peak lo Sp (Vo/20) x 1.414		Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.372	26.3mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P48	Serial No
Test EngineerXe	en	
Date27	'/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	2.00	2.8	141.4mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.1	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.69	2.4	119.5mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ	P48	Serial No
Test Engineer	.Xen	-	
Date	24/9/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch2	-143.5	-93.7	-153.7	20.7	$\checkmark$
Ch3	-143.5	-93.6	-153.6	20.9	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ48P....Serial No ..... Test Engineer ......RMC Date .....1/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ48P
Driver board ID	TACQ48P
Driver board Drawing No/Issue No	D0901048_V4
Monitor board ID	MON261
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

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Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ49..... Monitor Card ID....Mon243....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P49.....Serial No..... Test Engineer....Xen.... Date......13/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P49.....Serial No..... Test Engineer....Xen.... Date......10/9/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P49	Serial No	
Test Engineer	.Xen	-		
	40/0/40			

Date.....10/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P49.....Serial No..... Test Engineer....Xen.... Date......10/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P49	Serial No
Test Engineer	.Xen	
Date	.10/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P49	Serial No
Test Engineer	.Xen	
Date	.10/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

## **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.63	2.9µV√Hz	$\checkmark$
2		1.87	2.9µV√Hz	$\checkmark$
3		1.98	2.9µV√Hz	$\checkmark$
4		1.93	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P49	Serial No
Test Engineer	.Xen	
Date	.10/9/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P49.....Serial No..... Test Engineer....Xen.... Date......10/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

## **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P49	.Serial No
Test Engineer	Xen		
Date	13/9/10		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P49	.Serial No
Test Engineer	Xen	-	
Date	13/9/10.		

## **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T_ACQ_	P49	.Serial No
Test Engineer	.Xen		
Date	10/9/10		

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch2	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch3	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch4	-143.5	-91.0	-151.0	28.2	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ49P.....Serial No ..... Test Engineer ......RMC Date ......1/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ49P
Driver board ID	TACQ49
Driver board Drawing No/Issue No	DO901047_V4
Monitor board ID	MON243
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen..... Date......9/9/10.....

Drive Card ID.....T\_ACQ50..... Monitor Card ID....Mon242....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen..... Date......9/9/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen..... Date......9/9/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen..... Date......9/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P50	Serial No
Test Engineer	Xen	
Date	.9/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P50	Serial No
Test Engineer	.Xen	
Date	.9/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

## **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.71	2.9µV√Hz	$\checkmark$
2		1.69	2.9µV√Hz	$\checkmark$
3		1.63	2.9µV√Hz	$\checkmark$
4		1.70	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P50	Serial No
Test Engineer	Xen	
Date	.9/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P50.....Serial No..... Test Engineer....Xen..... Date......9/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

## **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P50	Serial No	
Test Engineer	Xen		
Date	9/9/10		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	12mV	600uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

# 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P50	.Serial No
Test Engineer	.Xen	-	
Date	.9/9/10		

## **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	.T_ACQ_P50	Serial No
Test Engineer	.Xen	
Date	.9/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch2	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-94.6	-154.6	18.6	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ50P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ50P
Driver board ID	TACQ50
Driver board Drawing No/Issue No	D0901047_5_K
Monitor board ID	MON242
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ51..... Monitor Card ID...Mon152.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
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- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P51	Serial No
Test Engineer	.Xen		
Data	20/0/40		

Date......30/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P51	Serial No
Test Engineer	.Xen	
Date	.30/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P51	Serial No
Test Engineer	.Xen	
Date	.30/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

## **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.36	2.9µV√Hz	$\checkmark$
2		1.69	2.9µV√Hz	$\checkmark$
3		1.53	2.9µV√Hz	$\checkmark$
4		1.67	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P51	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

## **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
Unit	T ACQ P51	Serial No		
---------------	-----------	-----------		
Test Engineer	.Xen			
Date	1/10/10			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.243	17.2mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	_ACQ_F	°51	.Serial No
Test Engineer>	(en		
Date1	/10/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P51	Serial No
Test Engineer	Xen	
Date	.30/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.2	-151.2	27.5	$\checkmark$
Ch2	-143.5	-93.6	-153.6	20.9	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-92.7	-152.7	23.2	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ51P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ51P
Driver board ID	TACQ51
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON152
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P52.....Serial No..... Test Engineer....Xen.... Date.......30/9/10.....

Drive Card ID.....T\_ACQ52..... Monitor Card ID...Mon192.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P	52Serial No
Test Engine	erXen	
<b>D</b> (	00/0//0	

Date......30/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P52	Serial No
Test Engineer	Xen	
Date	.30/9/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P52	Serial No
Test Engineer	.Xen	
Date	.30/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.63	2.9µV√Hz	$\checkmark$
2		1.53	2.9µV√Hz	$\checkmark$
3		1.65	2.9µV√Hz	$\checkmark$
4		1.30	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P52	Serial No
Test Engineer	.Xen		
Date	.30/9/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P52	.Serial No
Test Engineer	.Xen	-	
Date	.30/9/10.		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P	52Serial No	
Test EngineerX	en		
Date30	)/9/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ P52	Serial No
Test Engineer	.Xen	
Date	30/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch3	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch4	-143.5	-92.6	-152.6	23.4	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ52P....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ52P
Driver board ID	TACQ52
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON192
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ53..... Monitor Card ID...Mon228....

## **Contents**

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P53.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P53.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P53	Serial No	
Test Engineer	.Xen	-		
Data	4010140			

Date.....16/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P53.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P53	Serial No
Test Engineer	.Xen	
Date	16/8/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P53	Serial No
Test Engineer	.Xen	
Date	.16/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.96	2.9µV√Hz	$\checkmark$
2		1.83	2.9µV√Hz	$\checkmark$
3		1.97	2.9µV√Hz	$\checkmark$
4		1.85	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P53	Serial No
Test Engineer	.Xen		
Date	16/8/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P53.....Serial No..... Test Engineer....Xen..... Date......16/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch2	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P53	.Serial No
Test Engineer	.Xen	-	
Date	16/8/10.		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.239	16.9mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	Г_ACQ_Р53	Serial No	
Test Engineer	Ken		
Date1	6/8/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	$\checkmark$
Ch2	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch3	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch4	1.66	2.3	117.4mA	>125mA peak	$\checkmark$

Unit	.T_ACQ	P53	Serial No
Test Engineer	Xen	-	
Date	.16/8/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ53P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ53P
Driver board ID	TACQ53
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON226
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P54.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

Drive Card ID.....T\_ACQ54..... Monitor Card ID....Mon222....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P54.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P54.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P54	Serial No	
Test Engineer	.Xen	•		
D-4-	40/0/40			

Date.....16/8/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P54.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

#### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P54	Serial No
Test Engineer	.Xen	
Date	16/8/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P54	Serial No
Test Engineer	.Xen	
Date	16/8/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.74	2.9µV√Hz	$\checkmark$
2		1.66	2.9µV√Hz	$\checkmark$
3		1.66	2.9µV√Hz	$\checkmark$
4		1.68	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P54	Serial No
Test Engineer	Xen	
Date	.16/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P54.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P54	.Serial No
Test Engineer	Xen		
Date	16/8/10		

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.134	9.5mA	>2.5mA peak	$\checkmark$
Ch3	0.124	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.124	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.251	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.239	16.9mA	>2.5mA peak	$\checkmark$
Ch4	0.239	16.9mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ_P	°54	Serial No
Test Engineer	Xen		
Date1	16/8/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P54	.Serial No
Test Engineer	.Xen	
Date	.16/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-93.5	-153.5	21.1	$\checkmark$
Ch3	-143.5	-93.4	-153.4	21.4	$\checkmark$
Ch4	-143.5	-94.2	-154.2	19.5	$\checkmark$

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ54P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ54P
Driver board ID	TACQ54P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON222
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P55.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

Drive Card ID.....T\_ACQ55..... Monitor Card ID....Mon181.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P55.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P55.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P55	Serial No	
Test Engineer	.Xen	-		
Data	04/0/40			

Date.....24/8/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P55.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P55	.Serial No
Test Engineer	.Xen		
Date	24/8/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ	P55	Serial No
Test Engineer	.Xen	•	
Date	24/8/10		

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

#### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

#### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.94	2.9µV√Hz	$\checkmark$
2		1.34	2.9µV√Hz	$\checkmark$
3		1.39	2.9µV√Hz	$\checkmark$
4		1.19	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P55	Serial No
Test Engineer	Xen	-	
Date	.24/8/10.		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P55.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P55	Serial No
Test Engineer	.Xen	-	
Date	.24/8/10.		

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.120	8.5mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.233	16.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.367	25.9mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P55	.Serial No
Test Engineer>	(en	-	
Date2	4/8/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.95	2.8	137.9mA	>125mA peak	$\checkmark$
Ch4	1.95	2.8	137.9mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.65	2.3	116.7mA	>125mA peak	

Unit	.T_ACQ	P55	Serial No
Test Engineer	.Xen	-	
Date	.24/8/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.8	-153.8	20.4	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch4	-143.5	-91.5	-151.5	26.6	$\checkmark$

#### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ55P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ55P
Driver board ID	TACQ55
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON181
Monitor board Drawing No/Issue No	D0700480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P56.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

Drive Card ID.....T\_ACQ56.... Monitor Card ID...Mon191....

#### Contents

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- 3 Inspection
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- 6 Power
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- 8 Monitor Outputs
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- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P56.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P56.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_	P56	Serial No	
Test Engineer	.Xen	-		
Data	04/0/40			

Date.....24/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P56.....Serial No..... Test Engineer....Xen.... Date......24/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P56	Serial No
Test Engineer	.Xen	-	
Date	24/8/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ	P56	.Serial No
Test Engineer	.Xen		
Date	24/8/10		

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	
4	1.97	10	1.86v dc	

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.11	2.9µV√Hz	$\checkmark$
2		0.83	2.9µV√Hz	$\checkmark$
3		1.05	2.9µV√Hz	$\checkmark$
4		1.51	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P56	Serial No
Test Engineer	.Xen	-	
Date	.24/8/10.		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P56.....Serial No..... Test Engineer....Xen..... Date......24/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P56	.Serial No
Test Engineer	.Xen	-	
Date	.24/8/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.121	8.6mA	>2.5mA peak	$\checkmark$
Ch3	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.235	16.6mA	>2.5mA peak	$\checkmark$
Ch3	0.240	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P56	.Serial No
Test Engineer	Xen	-	
Date	24/8/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P56	.Serial No
Test Engineer	.Xen	-	
Date	24/8/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch4	-143.5	-91.6	-151.6	26.3	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ56P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ56P
Driver board ID	TACQ56
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON191
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. No

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ57..... Monitor Card ID....Mon140.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P57.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P57.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P57	Serial No	
Test Engineer	.Xen	-		
	44140140			

Date.....11/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P57.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P57	.Serial No
Test Engineer	.Xen	
Date	.11/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P57	Serial No
Test Engineer	Xen	
Date	.11/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.56	2.9µV√Hz	$\checkmark$
2		1.41	2.9µV√Hz	$\checkmark$
3		1.48	2.9µV√Hz	$\checkmark$
4		1.56	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P57	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P57	Serial No
Test EngineerX	en	
Date1	1/10/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.134	9.5mA	>2.5mA peak	$\checkmark$
Ch4	0.122	8.6mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.251	17.7mA	>2.5mA peak	$\checkmark$
Ch4	0.236	16.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P57	Serial No
Test EngineerXe	en	
Date11	/10/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ_P57	Serial No
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### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch2	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-90.9	-150.9	28.5	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ57P.....Serial No ..... Test Engineer ......RMC Date ......2/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ57P
Driver board ID	TACQ57P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON140
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P58.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

Drive Card ID.....T\_ACQ58..... Monitor Card ID....Mon257....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P58.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P58.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P58	Serial No	
Test Engineer	Xen	-		
Data	00/0/40			

Date.....23/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P58.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	T ACQ	P58	.Serial No
Test Engineer	.Xen		
Date	.23/9/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P58	Serial No
Test Engineer	.Xen	
Date	.23/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.46	2.9µV√Hz	$\checkmark$
2		1.38	2.9µV√Hz	$\checkmark$
3		1.75	2.9µV√Hz	$\checkmark$
4		1.50	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P58	Serial No
Test Engineer	.Xen	-	
Date	.23/9/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P58.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P58	.Serial No
Test Engineer	.Xen	-	
Date	.23/9/10.		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specificatio (Vo/20) x 1.414		Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P58	.Serial No
Test Engineer	Xen	-	
Date	23/9/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ	P58	.Serial No
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Date	.23/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.6	-151.6	26.3	$\checkmark$
Ch2	-143.5	-93.2	-153.2	21.9	$\checkmark$
Ch3	-143.5	-90.4	-150.4	30.2	$\checkmark$
Ch4	-143.5	-92.9	-152.9	22.6	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TACQ58P.....Serial No ..... Test Engineer ......RMC Date ......3/11/10√

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ58P
Driver board ID	TACQ58P
Driver board Drawing No/Issue No	D0901047_v4
Monitor board ID	MON257
Monitor board Drawing No/Issue No	D070480_5_K

### 9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ59..... Monitor Card ID...Mon258.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P59.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P59.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P59	Serial No	
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	00/0/40			

Date.....23/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P59.....Serial No..... Test Engineer....Xen.... Date......23/9/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P59	.Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ I	P59	.Serial No
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## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.93	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.97	1	1.86v dc	
2	1.97	4	1.86v dc	
3	1.97	7	1.86v dc	
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.31	2.9µV√Hz	$\checkmark$
2		1.71	2.9µV√Hz	$\checkmark$
3		1.60	2.9µV√Hz	$\checkmark$
4		1.68	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P59	Serial No
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## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P59.....Serial No..... Test Engineer....Xen.... Date......24/9/10....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P59	.Serial No
Test Engineer	.Xen	-	
Date	24/9/10.		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.134	9.5mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.250	17.7mA	>2.5mA peak	$\checkmark$
Ch2	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.251	17.7mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P59	.Serial No
Test Engineer>	(en	-	
Date2	4/9/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.99	2.8	140.7mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ	P59	Serial No
Test Engineer	.Xen	-	
Date	.23/9/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch2	-143.5	-91.9	-151.9	25.4	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-93.8	-153.8	20.4	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ59.....Serial No ..... Test Engineer ......RMC Date ......3/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ59P
Driver board ID	TACQ59P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON258
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\checkmark$
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ60..... Monitor Card ID....Mon158....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P60.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P60.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P60	Serial No	
Test Engineer	Xen	-		
Dete	1/10/10			

Date.....1/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P60.....Serial No..... Test Engineer....Xen..... Date......1/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P60	Serial No
Test Engineer	.Xen	-	
Date	1/10/10.		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P60	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.35	2.9µV√Hz	$\checkmark$
2		1.65	2.9µV√Hz	$\checkmark$
3		1.51	2.9µV√Hz	$\checkmark$
4		1.53	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P60	Serial No
Test Engineer	.Xen		
Date	.1/10/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$
Unit	T ACQ	P60	.Serial No	
---------------	----------	-----	------------	
Test Engineer	Xen	-		
Date	1/10/10.			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	13mV	650uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P60	Serial No
Test EngineerXe	en	-	
Date1/1	10/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T ACQ	P60	.Serial No
Test Engineer	.Xen		
Date	1/10/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch2	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch3	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch4	-143.5	-91.6	-151.6	26.3	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ60P[....Serial No ..... Test Engineer ......RMC Date ......3/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\checkmark$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ60P
Driver board ID	TACQ60
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON158
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P61.....Serial No..... Test Engineer....Xen..... Date......23/6/10.....

Drive Card ID.....T\_ACQ61P.... Monitor Card ID...Mon207....

## Contents

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- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P61.....Serial No..... Test Engineer....Xen.... Date......23/6/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	.T ACQ P61	Serial No
Test Engineer	Xen	
Date	.23/6/10	

# 3. Inspection

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Links: Check that the links W2 and W4 are present on each channel.

Unit1	_ACQ_	_P61	Serial No
Test Engineer>	(en		

Date......23/6/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P61.....Serial No..... Test Engineer....Xen..... Date......23/6/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P61	Serial No
Test Engineer	.Xen	
Date	23/6/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P61	Serial No
Test Engineer	.Xen	
Date	.23/6/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.25	2.9µV√Hz	$\checkmark$
2		1.29	2.9µV√Hz	$\checkmark$
3		0.82	2.9µV√Hz	$\checkmark$
4		1.11	2.9µV√Hz	$\checkmark$

Unit	T ACQ P61	Serial No
Test Engineer	Xen	
Date	23/6/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P61.....Serial No..... Test Engineer....Xen..... Date......23/6/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch2	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch3	65mV	3.3mA	>2.5mA peak	$\checkmark$
Ch4	65mV	3.3mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.064	4.5mA	>2.5mA peak	$\checkmark$
Ch2	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch3	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch4	0.064	4.5mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P6	1Serial No
Test EngineerX	en	
Date23	<u>3/6/10</u>	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.134	9.5mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.132	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.252	17.8mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.249	17.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P61	.Serial No
Test EngineerX	en	•	
Date23	3/6/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.7	2.4	120.2mA	>125mA peak	
Ch2	1.7	2.4	120.2mA	>125mA peak	
Ch3	1.7	2.4	120.2mA	>125mA peak	
Ch4	1.7	2.4	120.2mA	>125mA peak	

Unit	.T_ACQ_P61	Serial No	
Test Engineer	.Xen		
Date	.23/6/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch2	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch3	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch4	-143.5	-92.2	-152.2	24.5	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ61P.....Serial No ..... Test Engineer ......RMC Date ......3/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ61P
Driver board ID	TACQ61P
Driver board Drawing No/Issue No	D0901047
Monitor board ID	MON207
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P62.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

Drive Card ID.....T\_ACQ62..... Monitor Card ID....Mon163.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P62.....Serial No..... Test Engineer....Xen.... Date......16/8/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P62....Serial No.... Test Engineer....Xen.... Date......13/8/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P62	Serial No
Test Engineer	Xen	-	
	40/0/40		

Date.....13/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P62.....Serial No..... Test Engineer....Xen..... Date......13/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P	62	.Serial No
Test Engineer	.Xen		
Date	13/8/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P62	Serial No
Test Engineer	.Xen	
Date	.13/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.35	2.9µV√Hz	$\checkmark$
2		0.90	2.9µV√Hz	$\checkmark$
3		1.21	2.9µV√Hz	$\checkmark$
4		1.14	2.9µV√Hz	$\checkmark$

Unit	T ACQ P	62	.Serial No
Test Engineer	.Xen		
Date	.16/8/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P62.....Serial No..... Test Engineer....Xen..... Date......16/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P62	.Serial No
Test Engineer	.Xen	-	
Date	16/8/10.		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch2	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.124	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.125	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.239	16.9mA	>2.5mA peak	$\checkmark$
Ch4	0.240	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ F	P62	Serial No
Test Engineer	Xen		
Date1	16/8/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P62	.Serial No
Test Engineer	.Xen	-	
Date	16/8/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch2	-143.5	-93.1	-153.3	21.6	$\checkmark$
Ch3	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch4	-143.5	-93.4	-153.4	21.4	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit......TACQ62P√.....Serial No ..... Test Engineer ......RMC Date ......3/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\checkmark$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ62P
Driver board ID	TACQ62
Driver board Drawing No/Issue No	DD0901047_V4
Monitor board ID	MON163
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P63.....Serial No..... Test Engineer....Xen.... Date......13/8/10....

Drive Card ID.....T\_ACQ63..... Monitor Card ID....Mon161....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P63.....Serial No..... Test Engineer....Xen.... Date......13/8/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P63.....Serial No..... Test Engineer....Xen.... Date......13/8/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P63	Serial No	
Test Engineer	.Xen	-		
Data	40/0/40			

Date.....13/8/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P63.....Serial No..... Test Engineer....Xen.... Date......13/8/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P63	.Serial No
Test Engineer	.Xen	-	
Date	13/8/10.		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P63	Serial No
Test Engineer	.Xen	
Date	.13/8/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.99	2.9µV√Hz	$\checkmark$
2		0.76	2.9µV√Hz	$\checkmark$
3		0.95	2.9µV√Hz	$\checkmark$
4		1.18	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P63	Serial No
Test Engineer	.Xen	-	
Date	.13/8/10.		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P63.....Serial No..... Test Engineer....Xen..... Date......13/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P63	Serial No
Test Engineer	.Xen	-	
Date	13/8/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.120	8.5mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.233	16.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P63	Serial No
Test Engineer	.Xen	-	
Date	13/8/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ	P63	Serial No
Test Engineer	.Xen	-	
Date	13/8/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch2	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ63P.....Serial No ..... Test Engineer ......RMC Date ......3/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\checkmark$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\checkmark$
- 7. Check that all links W4 are in place.  $\checkmark$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ63P
Driver board ID	TACQ63
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON161
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect. . √
- 11. Put the lid on and fasten all screws,  $\checkmark$

Check all external screws for tightness.  $\checkmark$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P64.....Serial No..... Test Engineer....Xen.... Date......30/9/10....

Drive Card ID.....T\_ACQ64..... Monitor Card ID...Mon219.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P64.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_	P64	Serial No	
Test Engineer	.Xen	-		
Data	00/0/40			

Date.....29/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P64.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P64	Serial No
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## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P64	Serial No
Test Engineer	.Xen	
Date	.29/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.47	2.9µV√Hz	$\checkmark$
2		1.43	2.9µV√Hz	$\checkmark$
3		1.32	2.9µV√Hz	$\checkmark$
4		1.14	2.9µV√Hz	$\checkmark$

Unit	T ACQ I	P64	Serial No
Test Engineer	.Xen		
Date	.29/9/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P64.....Serial No..... Test Engineer....Xen.... Date......30/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P64	.Serial No
Test EngineerX	en		
Date30	)/9/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.131	9.3mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.248	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	L_ACQ	P64	.Serial No
Test Engineer>	Ken	-	
Date3	80/9/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ_P	64	Serial No
Test Engineer	.Xen		
Date	.29/9/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.8	-153.8	20.4	$\checkmark$
Ch2	-143.5	-91.9	-151.9	25.4	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-91.7	-151.7	26.0	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ64P....Serial No ..... Test Engineer ......RMC Date ......3/11.10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ64P
Driver board ID	TACQ64P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON219
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P65.....Serial No..... Test Engineer....Xen.... Date.......30/9/10.....

Drive Card ID.....T\_ACQ65..... Monitor Card ID....Mon179.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T_ACQ	P65	Serial No
Test Engineer	Xen	-	
	00/0/40		

Date......30/9/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P65	Serial No
Test Engineer	.Xen	-	
Date	.30/9/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ	P65	.Serial No
Test Engineer	.Xen	•	
Date	30/9/10.		

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.44	2.9µV√Hz	$\checkmark$
2		1.32	2.9µV√Hz	$\checkmark$
3		1.27	2.9µV√Hz	$\checkmark$
4		1.71	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P65	Serial No
Test Engineer	.Xen	-	
Date	.30/9/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P65	.Serial No
Test Engineer	.Xen	-	
Date	.30/9/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P65	.Serial No
Test Engineer	Xen	-	
Date	30/9/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T_ACQ	P65	.Serial No
Test Engineer	.Xen	-	
Date	30/9/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch2	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch3	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch4	-143.5	-91.7	-151.7	26.0	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ65P....Serial No ..... Test Engineer ......RMC Date ......3/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ65P
Driver board ID	TACQ65P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON179
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P66.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

Drive Card ID.....T\_ACQ66..... Monitor Card ID...Mon240.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
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- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
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- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P66.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P66.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P66	Serial No	
Test Engineer	.Xen	-		
Data	4140140			

Date.....4/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P66.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P66	Serial No
Test Engineer	.Xen	-	
Date	.4/10/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ	P66	.Serial No
Test Engineer	.Xen	•	
Date	4/10/10.		

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.76	2.9µV√Hz	$\checkmark$
2		1.74	2.9µV√Hz	$\checkmark$
3		1.76	2.9µV√Hz	$\checkmark$
4		1.96	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P66	Serial No
Test Engineer	.Xen	-	
Date	.4/10/10.		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P66.....Serial No..... Test Engineer....Xen..... Date......4/10/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P66	.Serial No
Test Engineer	.Xen	-	
Date	.4/10/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	13mV	650uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.121	8.6mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.235	16.6mA	>2.5mA peak	$\checkmark$
Ch3	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P66	.Serial No
Test Engineer	Xen	-	
Date	4/10/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ	P66	.Serial No
Test Engineer	.Xen	-	
Date	4/10/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch2	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ66P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ66P
Driver board ID	TACQ66P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON240
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect. √
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P67.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

Drive Card ID.....T\_ACQ67..... Monitor Card ID...Mon239.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P67.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P67	Serial No	
Test Engineer	.Xen	-		
Data	4140140			

Date.....4/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P67.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	T ACQ	P67	Serial No
Test Engineer	.Xen	-	
Date	4/10/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ	P67	.Serial No
Test Engineer	.Xen	•	
Date	.4/10/10		

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.62	2.9µV√Hz	$\checkmark$
2		1.54	2.9µV√Hz	$\checkmark$
3		1.68	2.9µV√Hz	$\checkmark$
4		1.87	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P67	Serial No
Test Engineer	.Xen	-	
Date	.4/10/10.		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P67.....Serial No..... Test Engineer....Xen.... Date......4/10/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P67	.Serial No
Test Engineer	.Xen	-	
Date	4/10/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

Unit	L_ACQ	P67	.Serial No
Test Engineer	Ken	-	
Date4	/10/10.		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ	P67	Serial No
Test Engineer	.Xen	-	
Date	4/10/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch2	-143.5	-91.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch4	-143.5	-93.2	-153.2	21.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ67P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ67P
Driver board ID	TACQ67P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON239
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ68..... Monitor Card ID....Mon205....

### **Contents**

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P68.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P68.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P	68Serial No
Test Engineer	Xen	
<b>n</b> (		

Date.....11/10/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P68.....Serial No..... Test Engineer....Xen..... Date......11/10/10.....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P68	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

### **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P68	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.93	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.09	2.9µV√Hz	$\checkmark$
2		1.56	2.9µV√Hz	$\checkmark$
3		1.17	2.9µV√Hz	$\checkmark$
4		0.95	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P68	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ F	P68	Serial No
Test Engineer>	(en		
Date1	1/10/10.		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.118	8.3mA	>2.5mA peak	$\checkmark$
Ch2	0.123	8.7mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.231	16.3mA	>2.5mA peak	$\checkmark$
Ch2	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P68	.Serial No
Test Engineer	Xen	-	
Date	11/10/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P68	Serial No
Test Engineer	.Xen	
Date	.11/10/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch2	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch3	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch4	-143.5	-93.3	-153.3	21.6	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ68P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ68P
Driver board ID	TACQ68P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON205
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P69.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

Drive Card ID.....T\_ACQ69..... Monitor Card ID....Mon177.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P69.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P69.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ	P69	Serial No	
Test Engineer	.Xen	-		
Data	00/0/40			

Date.....29/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		$\checkmark$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P69.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ	P69	.Serial No
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## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	T ACQ P69	Serial No
Test Engineer	.Xen	
Date	29/9/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.90	5	1.86v r.m.s	$\checkmark$
3	1.90	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.93	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.33	2.9µV√Hz	$\checkmark$
2		1.41	2.9µV√Hz	$\checkmark$
3		1.45	2.9µV√Hz	$\checkmark$
4		1.61	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P69	.Serial No
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Date	.29/9/10		

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P69.....Serial No..... Test Engineer....Xen.... Date......29/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
Unit	T ACQ	P69	.Serial No	
---------------	-----------	-----	------------	
Test Engineer	.Xen	-		
Date	.29/9/10.			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T_ACQ	P69	.Serial No
Test Engineer	Xen	-	
Date	29/9/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T_ACQ_	P69	.Serial No
Test Engineer	.Xen	-	
Date	29/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-94.5	-154.5	18.8	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ69P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ69P
Driver board ID	TACQ69P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON177
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ70..... Monitor Card ID....Mon197.....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P70.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit	.T ACQ P70	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

# 3. Inspection

# Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P70	Serial No	
Test Engineer	Xen	-		
Dete	1/10/10			

Date.....1/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\checkmark$
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P70.....Serial No..... Test Engineer....Xen..... Date......1/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P70	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P70	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.93	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.97	4	1.86v dc	
3	1.95	7	1.86v dc	$\checkmark$
4	1.97	10	1.86v dc	

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.44	2.9µV√Hz	$\checkmark$
2		1.30	2.9µV√Hz	$\checkmark$
3		1.27	2.9µV√Hz	$\checkmark$
4		1.18	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P70	Serial No
Test Engineer	Xen	
Date	.1/10/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.065	4.6mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.320	22.6mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P70	Serial No
Test Engineer	Xen	
Date	1/10/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	12mV	600uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch2	0.120	8.5mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.124	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch2	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.239	16.9mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P	70	Serial No
Test Engineer	Xen		
Date	1/10/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	138.6mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P70	Serial No	
Test Engineer	.Xen		
Date	.1/10/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch2	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch3	-143.5	-93.6	-153.6	20.9	$\checkmark$
Ch4	-143.5	-93.1	-153.1	22.1	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ70P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ70P
Driver board ID	TACQ70P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON197
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ71..... Monitor Card ID...Mon253.....

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- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P71.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P71.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

# 3. Inspection

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

IC2 and IC4 (AD8671) have been replaced on CH1 due to being too noisy.

#### Links:

Check that the links W2 and W4 are present on each channel.

Unit	T ACQ	P71	Serial No	
Test Engineer	Xen	-		
Dete	1/10/10			

Date.....1/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P71.....Serial No..... Test Engineer....Xen.... Date......1/10/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P71	Serial No
Test Engineer	Xen	
Date	.1/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P71	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (µV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.59	2.9µV√Hz	$\checkmark$
2		1.42	2.9µV√Hz	$\checkmark$
3		1.31	2.9µV√Hz	$\checkmark$
4		1.52	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P71	Serial No
Test Engineer	Xen	
Date	.1/10/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.325	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.391	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	Г ACQ Р71	Serial No
Test Engineer>	Ken	
Date1	/10/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	16mV	700uA	>2.5mA peak	
Ch4	13mV	650uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.123	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.238	16.8mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.243	17.2mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P71	Serial No
Test Engineer	.Xen	
Date	.1/10/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.96	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ F	71	Serial No	
Test Engineer	.Xen			
Date	.1/10/10			

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-92.0	-152.0	25.1	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ71P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ71P
Driver board ID	TACQ71
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON253
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ72..... Monitor Card ID...Mon235.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P72.....Serial No..... Test Engineer....Xen..... Date......13/10/10.....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P72.....Serial No..... Test Engineer....Xen..... Date......13/10/10.....

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

UnitT_A	ACQ_F	۶ <mark>72</mark>	Serial No
Test EngineerXer	<b>۱</b>		

Date......13/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P72.....Serial No..... Test Engineer....Xen..... Date......13/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P72	Serial No
Test Engineer	.Xen	
Date	.13/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P72	Serial No
Test Engineer	.Xen	
Date	.13/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.57	2.9µV√Hz	$\checkmark$
2		1.66	2.9µV√Hz	$\checkmark$
3		1.30	2.9µV√Hz	$\checkmark$
4		1.45	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P72	Serial No
Test Engineer	.Xen	
Date	.13/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P72.....Serial No..... Test Engineer....Xen.... Date......13/10/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P72	Serial No
Test EngineerX	en	
Date13	3/10/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.122	8.6mA	>2.5mA peak	$\checkmark$
Ch4	0.125	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.237	16.8mA	>2.5mA peak	$\checkmark$
Ch4	0.240	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P72	Serial No
Test Engineer	Xen	
Date	13/10/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	137.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T ACQ P72	Serial No
Test Engineer	Xen	
Date	.13/10/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-91.2	-151.2	27.5	$\checkmark$
Ch3	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch4	-143.5	-91.9	-151.9	25.4	$\checkmark$

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ72P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ72P
Driver board ID	TACQ73
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON235
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ73..... Monitor Card ID...Mon64....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P73.....Serial No..... Test Engineer....Xen..... Date......12/10/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

# **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\checkmark$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Replaced J6 on the Driver board.

#### Links:

Check that the links W2 and W4 are present on each channel.

Test Engineer Von	UnitT_ACQ	P73	Serial No	
rest Engineer	Test EngineerXen	_		

Date.....12/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P73.....Serial No..... Test Engineer....Xen..... Date......12/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P73	Serial No
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Date	.12/10/10	

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P73	Serial No
Test Engineer	.Xen	
Date	.12/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	2	1.86v r.m.s	$\checkmark$
2	1.94	5	1.86v r.m.s	$\checkmark$
3	1.94	8	1.86v r.m.s	$\checkmark$
4	1.94	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.98	1	1.86v dc	
2	1.98	4	1.86v dc	
3	1.97	7	1.86v dc	
4	1.97	10	1.86v dc	

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.05	2.9µV√Hz	$\checkmark$
2		1.27	2.9µV√Hz	$\checkmark$
3		1.76	2.9µV√Hz	$\checkmark$
4		1.88	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P73	Serial No
Test Engineer	.Xen	
Date	.12/10/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.388	27.4mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P73	Serial No
Test EngineerX	en	
Date1	2/10/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak Io (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	12mV	600uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.117	8.3mA	>2.5mA peak	$\checkmark$
Ch2	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.125	8.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.230	16.3mA	>2.5mA peak	$\checkmark$
Ch2	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.240	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.367	25.9mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P73	Serial No
Test EngineerX	en	
Date12	2/10/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.65	2.3	116.7mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	T ACQ I	P73	Serial No
Test Engineer	.Xen		
Date	12/10/10		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.0	-151.0	28.2	$\checkmark$
Ch2	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch3	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch4	-143.5	-92.2	-152.2	24.5	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ73P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ73P
Driver board ID	TACQ73P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON64
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ74..... Monitor Card ID....Mon185....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P74.....Serial No..... Test Engineer....Xen.... Date......13/10/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P74.....Serial No..... Test Engineer....Xen.... Date......13/10/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T_ACQ_P74	Serial No
Test Engine	erXen	
<b>D</b> (	10/10/10	

Date.....13/10/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit.....T\_ACQ\_P74.....Serial No..... Test Engineer....Xen.... Date......13/10/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

# If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P74	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P74	Serial No
Test Engineer	.Xen	
Date	.13/10/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.98	2.9µV√Hz	$\checkmark$
2		1.48	2.9µV√Hz	$\checkmark$
3		1.02	2.9µV√Hz	$\checkmark$
4		1.77	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P74	Serial No
Test Engineer	.Xen	
Date	.13/10/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P74.....Serial No..... Test Engineer....Xen.... Date......13/10/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P74	Serial No
Test EngineerXe	en	
Date13	3/10/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch2	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.124	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.240	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P74	Serial No
Test Engineer	.Xen	
Date	.13/10/1080	DuA

# **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.68	2.4	118.8mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ F	٩٨٠٠٠٠٠	Serial No	
Test Engineer	.Xen			
Date	.13/10/10.			

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch2	-143.5	-93.9	-153.9	20.2	$\checkmark$
Ch3	-143.5	-91.3	-151.3	27.2	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ74P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ74P
Driver board ID	TACQ74P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON185
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

Drive Card ID.....T\_ACQ75..... Monitor Card ID...Mon196.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

# **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit.....Serial No..... Test Engineer..... Date.....

# 7. Relay Operation

Operate each relay in turn.

Observe its operation. LEDs should illuminate when the relays are operated.

# **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P75	Serial No
Test Engineer	.Xen	
Date	.2/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

# 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.80	2.9µV√Hz	$\checkmark$
2		1.23	2.9µV√Hz	$\checkmark$
3		0.92	2.9µV√Hz	$\checkmark$
4		1.20	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P75	Serial No
Test Engineer	Xen	
Date	.2/8/10	

# 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P75.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P75	Serial No
Test Engineer	Xen	
Date	.2/8/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

# 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	14mV	700uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.121	8.6mA	>2.5mA peak	$\checkmark$
Ch2	0.122	8.6mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.123	8.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.234	16.5mA	>2.5mA peak	$\checkmark$
Ch2	0.236	16.7mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.238	16.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s Peak lo (Vo/20) x 1.414		Specification	Pass/Fail
Ch1	0.368	26.0mA	>2.5mA peak	$\checkmark$
Ch2	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P75	Serial No
Test EngineerXe	en	
Date2/8	8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	140mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	140mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch2	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch3	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch4	1.67	2.4	118.1mA	>125mA peak	$\checkmark$

Unit	.T_ACQ_P75	Serial No
Test Engineer	Xen	
Date	.2/8/10	

# **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.4	-151.4	26.9	$\checkmark$
Ch2	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch3	-143.5	-92.0	-152.0	25.1	$\checkmark$
Ch4	-143.5	-94.0	-154.0	20.0	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ75P....Serial No ..... Test Engineer ......RMC Date ......8/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ75P
Driver board ID	TACQ75P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON196
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

10. Visually inspect.  $\sqrt{}$ 

11. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P76.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

Drive Card ID.....T\_ACQ76..... Monitor Card ID...Mon59....

## Contents

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- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit.....T\_ACQ\_P76.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P76.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\overline{\mathbf{A}}$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P76.....Serial No..... Test Engineer....Xen..... Date......30/7/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.
Unit	.T ACQ P76	Serial No
Test Engineer	Xen	
Date	.30/7/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P76	Serial No
Test Engineer	.Xen	
Date	.2/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.93	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.93	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.06	2.9µV√Hz	$\checkmark$
2		1.68	2.9µV√Hz	$\checkmark$
3		1.57	2.9µV√Hz	$\checkmark$
4		1.01	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P76	Serial No
Test Engineer	Xen	
Date	.2/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P76.....Serial No..... Test Engineer....Xen..... Date......2/8/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.067	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.321	22.7mA	>2.5mA peak	$\checkmark$
Ch4	0.325	23.0mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P76	Serial No
Test Engineer	Xen	
Date	.2/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch3	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch2	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch3	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch4	0.242	17.1mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo Specification (Vo/20) x 1.414		Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P76	Serial No
Test EngineerX	en	
Date2/8	8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	140mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch2	1.68	2.4	118.8mA	>125mA peak	$\checkmark$
Ch3	1.66	2.3	117.4mA	>125mA peak	$\checkmark$
Ch4	1.66	2.3	117.4mA	>125mA peak	$\checkmark$

Unit	T_ACQ_P76	Serial No
Test Engineer	.Xen	
Date	2/8/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch2	-143.5	-92.4	-152.4	24.0	$\checkmark$
Ch3	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch4	-143.5	-93.2	-153.2	21.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ76P.....Serial No ..... Test Engineer ......RMC Date ......8/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ76P
Driver board ID	TACQ76P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON59
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P77.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

Drive Card ID.....T\_ACQ77..... Monitor Card ID....Mon229....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P77.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P77.....Serial No..... Test Engineer....Xen.... Date.......26/8/10.....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T_ACQ_P77	Serial No
Test Engin	eer <mark>Xe</mark> n	
<b>D</b> /	00/0//0	

Date......26/8/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P77.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P77	Serial No
Test Engineer	Xen	
Date	.26/8/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P77	Serial No
Test Engineer	.Xen	
Date	.26/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.58	2.9µV√Hz	$\checkmark$
2		1.65	2.9µV√Hz	$\checkmark$
3		1.42	2.9µV√Hz	$\checkmark$
4		1.82	2.9µV√Hz	$\checkmark$

Unit	T ACQ P77	Serial No
Test Engineer	Xen	
Date	26/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P77.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.323	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P77	Serial No
Test Engineer>	Xen	
Date2	26/8/10	

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

### 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	16mV	800uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch2	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch3	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.126	8.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.251	17.7mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch4	0.241	17.0mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P77	Serial No
Test Engineer	.Xen	
Date	26/8/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P77	Serial No
Test Engineer	Xen	-	
Date	.26/8/10.		

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.4	-153.4	21.4	$\checkmark$
Ch2	-143.5	-92.2	-152.2	24.5	$\checkmark$
Ch3	-143.5	-93.1	-153.1	22.1	$\checkmark$
Ch4	-143.5	-92.4	-152.4	24.0	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ77P....Serial No ..... Test Engineer ......RMC Date ......8/11/10

### **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ77P
Driver board ID	TACQ77P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON229
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

10. Visually inspect.  $\sqrt{}$ 

11. Put the lid on and fasten all screws,  $\sqrt{}$ 

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P78.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

Drive Card ID.....T\_ACQ78..... Monitor Card ID....Mon230.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

### **Block diagram**



### Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P78.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

### 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77111	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P78.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T_ACQ_	278Serial No
Test Engineer	.Xen	
Data	05/0/40	

Date.....25/8/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P78.....Serial No..... Test Engineer....Xen.... Date......25/8/10....

### 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)	
500mA	400mA	

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P78	Serial No
Test Engineer	Xen	
Date	.25/8/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## **FILTER**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P78	Serial No
Test Engineer	.Xen	
Date	.25/8/10	

### 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

### 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.59	2.9µV√Hz	$\checkmark$
2		1.59	2.9µV√Hz	$\checkmark$
3		1.51	2.9µV√Hz	$\checkmark$
4		1.74	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P78	Serial No
Test Engineer	Xen	
Date	.26/8/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P78.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.065	4.6mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$
UnitT	ACQ P78	Serial No		
----------------	---------	-----------		
Test EngineerX	en			
Date26	6/8/10			

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	13mV	650uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	12mV	600uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.133	9.4mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.251	17.7mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P78	.Serial No
Test EngineerX	en	-	
Date26	/8/10.		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	T ACQ	P78	Serial No
Test Engineer	Xen	-	
Date	.26/8/10.		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.8	-151.8	25.7	$\checkmark$
Ch2	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch3	-143.5	-91.5	-151.5	26.6	$\checkmark$
Ch4	-143.5	-90.7	-150.7	29.2	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ78P....Serial No ..... Test Engineer ......RMC Date ......8/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ78P
Driver board ID	TACQ78P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON230
Monitor board Drawing No/Issue No	D0701047_V4

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen.... Date......6/9/10....

Drive Card ID.....T\_ACQ79..... Monitor Card ID....Mon231.....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen..... Date......6/9/10.....

# 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

# **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P79	Serial No
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# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P79	Serial No
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Date	.6/9/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.91	2	1.86v r.m.s	$\checkmark$
2	1.91	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.91	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.66	2.9µV√Hz	$\checkmark$
2		1.69	2.9µV√Hz	$\checkmark$
3		1.61	2.9µV√Hz	$\checkmark$
4		1.30	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P79	Serial No
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## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P79.....Serial No..... Test Engineer....Xen..... Date......6/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	.T ACQ P79	Serial No
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Date	.6/9/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.123	8.7mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch3	0.243	17.2mA	>2.5mA peak	$\checkmark$
Ch4	0.238	16.8mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P79	Serial No
Test EngineerXe	en	
Date6/9	9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.66	2.3	117.4mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	.T_ACQ_P79	Serial No
Test Engineer	Xen	
Date	.6/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch2	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-92.1	-152.1	24.8	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ79P.....Serial No ..... Test Engineer ......RMC Date ......8/10/11

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ78P
Driver board ID	TACQ78
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON231
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,

Check all external screws for tightness.

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm

# TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P80.....Serial No..... Test Engineer....Xen.... Date......6/9/10....

Drive Card ID.....T\_ACQ80..... Monitor Card ID....Mon232....

# Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- **10.3 Acquisition Mode**
- 11 Noise Measurements
- 12 Final Assembly Tests

# **1. Description**

# **Block diagram**



# Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P80.....Serial No..... Test Engineer....Xen.... Date......6/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P80.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

# **3. Inspection**

# Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	.T ACQ	P80	Serial No	
Test Engineer	Xen	-		
Data	00/0/40			

Date.....26/8/10.....

# **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

# LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\overline{\mathbf{v}}$

# **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

# 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P80.....Serial No..... Test Engineer....Xen.... Date......26/8/10....

# 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ F	°80	.Serial No
Test Engineer	.Xen		
Date	26/8/10		

# 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

# FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

# **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P80	Serial No
Test Engineer	.Xen	
Date	.26/8/10	

# 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.96	7	1.86v dc	$\checkmark$
4	1.96	10	1.86v dc	$\checkmark$

# 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.52	2.9µV√Hz	$\checkmark$
2		1.75	2.9µV√Hz	$\checkmark$
3		1.70	2.9µV√Hz	$\checkmark$
4		1.72	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P80	Serial No
Test Engineer	.Xen	
Date	.6/9/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P80.....Serial No..... Test Engineer....Xen.... Date......6/9/10....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P80	.Serial No
Test Engineer	.Xen	-	
Date	.6/9/10		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

## 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch3	0.246	17.4mA	>2.5mA peak	$\checkmark$
Ch4	0.247	17.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ F	P80Serial No
Test EngineerXe	en	
Date6/9	9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch3	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ P80	Serial No
Test Engineer	.Xen	
Date	6/9/10	

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-92.9	-152.9	22.6	$\checkmark$
Ch2	-143.5	-92.1	-152.1	24.8	$\checkmark$
Ch3	-143.5	-92.3	-152.3	24.3	$\checkmark$
Ch4	-143.5	-92.9	-152.9	22.6	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ80P.....Serial No ..... Test Engineer ......RMC Date ......4/11/10

# **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ80P
Driver board ID	TACQ80P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON232
Monitor board Drawing No/Issue No	D070480_V5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$
# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

Drive Card ID.....T\_ACQ81..... Monitor Card ID....Mon233.....

## Contents

- 1 Description
- 2 Test Equipment
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- 8.4 Noise Monitors
- 9. Distortion
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- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

## **3. Inspection**

### Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

### If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P81	Serial No
Test Engineer	.Xen	
Date	.6/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P81	Serial No
Test Engineer	.Xen	
Date	.6/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s.Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.95	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.44	2.9µV√Hz	$\checkmark$
2		1.36	2.9µV√Hz	$\checkmark$
3		1.87	2.9µV√Hz	$\checkmark$
4		1.47	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P81	Serial No
Test Engineer	.Xen	
Date	.6/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P81.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch3	0.323	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.414	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P81	Serial No
Test Engineer	Xen	
Date	7/9/10	

#### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	12mV	600uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	16mV	800uA	>2.5mA peak	

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.130	9.2mA	>2.5mA peak	$\checkmark$
Ch2	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch4	0.128	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch2	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.244	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P81	.Serial No
Test EngineerXe	en	
Date7/9	9/10	

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.98	2.8	140.0mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P81	Serial No
Test Engineer	.Xen	
Date	.6/9/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-91.7	-151.7	26.0	$\checkmark$
Ch2	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch3	-143.5	-92.7	-152.7	23.2	$\checkmark$
Ch4	-143.5	-90.9	-150.9	28.5	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ81P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ81P
Driver board ID	TACQ81P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON233
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

Drive Card ID.....T\_ACQ82..... Monitor Card ID....Mon234.....

### Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel. Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

#### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	
9	PD4N	Photodiode D-	17	$\checkmark$

### **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

### **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

#### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen..... Date.......6/9/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P82	Serial No
Test Engineer	Xen	
Date	.6/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T_ACQ_P82	Serial No
Test Engineer	.Xen	
Date	7/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

### 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S Monitor	Expected value	Pass/Fail: Equal? (+/- 0.1v)
1	0.33	3	0.33v	
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

#### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.90	2	1.86v r.m.s	$\checkmark$
2	1.90	5	1.86v r.m.s	$\checkmark$
3	1.91	8	1.86v r.m.s	$\checkmark$
4	1.90	11	1.86v r.m.s	$\checkmark$

### 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.94	1	1.86v dc	$\checkmark$
2	1.94	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.94	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.50	2.9µV√Hz	$\checkmark$
2		1.38	2.9µV√Hz	$\checkmark$
3		1.49	2.9µV√Hz	$\checkmark$
4		1.55	2.9µV√Hz	$\checkmark$

Unit	.T ACQ P82	Serial No
Test Engineer	Xen	
Date	.7/9/10	

### 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P82.....Serial No..... Test Engineer....Xen..... Date......7/9/10.....

#### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

#### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch2	0.327	23.1mA	>2.5mA peak	$\checkmark$
Ch3	0.322	22.8mA	>2.5mA peak	$\checkmark$
Ch4	0.322	22.8mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch2	0.392	27.7mA	>2.5mA peak	$\checkmark$
Ch3	0.389	27.5mA	>2.5mA peak	$\checkmark$
Ch4	0.388	27.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.413	29.2mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P82	.Serial No
Test Engineer	.Xen	-	
Date	.7/9/10		

### 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	15mV	750uA	>2.5mA peak	
Ch2	15mV	750uA	>2.5mA peak	
Ch3	15mV	750uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.126	8.9mA	>2.5mA peak	$\checkmark$
Ch2	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.125	8.8mA	>2.5mA peak	$\checkmark$
Ch4	0.129	9.1mA	>2.5mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.242	17.1mA	>2.5mA peak	$\checkmark$
Ch2	0.247	17.5mA	>2.5mA peak	$\checkmark$
Ch3	0.241	17.0mA	>2.5mA peak	$\checkmark$
Ch4	0.245	17.3mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch4	0.368	26.0mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P82	.Serial No
Test Engineer	.Xen	-	
Date	.7/9/10		

#### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

#### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch2	1.98	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

#### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.68	2.4	118.8mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.66	2.3	117.4mA	>125mA peak	

Unit	.T_ACQ_P82	Serial No
Test Engineer	.Xen	
Date	.7/9/10	

### **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



#### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-89.5	-149.5	33.5	$\checkmark$
Ch2	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch3	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch4	-143.5	-93.6	-153.6	20.9	

### Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ82P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ82P
Driver board ID	TACQ82P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON234
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ83..... Monitor Card ID....Mon249....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P83.....Serial No..... Test Engineer....Xen.... Date......17/9/10....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	
Unit......T\_ACQ\_P83.....Serial No..... Test Engineer....Xen.... Date......16/9/10....

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T_ACQ_	P83	Serial No	
Test Engineer	.Xen	-		
Data	40/0/40			

Date.....16/9/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## **LED Mon**

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\overline{\mathbf{v}}$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		
25	0V (TP3)		

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P83.....Serial No..... Test Engineer....Xen.... Date......16/9/10....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	.T ACQ P83	Serial No
Test Engineer	.Xen	
Date	.16/9/10	

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P83	Serial No
Test Engineer	.Xen	
Date	.16/9/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.95	4	1.86v dc	$\checkmark$
3	1.95	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		1.30	2.9µV√Hz	$\checkmark$
2		1.90	2.9µV√Hz	$\checkmark$
3		1.60	2.9µV√Hz	$\checkmark$
4		1.46	2.9µV√Hz	$\checkmark$

Unit	T ACQ	P83	Serial No
Test Engineer	.Xen		
Date	16/9/10		

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

Unit......T\_ACQ\_P83.....Serial No..... Test Engineer....Xen.... Date......17/9/10.....

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.324	22.9mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.390	27.6mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.416	29.4mA	>2.5mA peak	$\checkmark$
Ch3	0.415	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ P83	Serial No
Test Engineer	.Xen	
Date	17/9/10	

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	14mV	700uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	14mV	700uA	>2.5mA peak	
Ch4	14mV	700uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.127	9.0mA	>2.5mA peak	$\checkmark$
Ch3	0.129	9.1mA	>2.5mA peak	$\checkmark$
Ch4	0.130	9.2mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch3	0.245	17.3mA	>2.5mA peak	$\checkmark$
Ch4	0.246	17.4mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.369	26.1mA	>2.5mA peak	$\checkmark$
Ch2	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.370	26.2mA	>2.5mA peak	$\checkmark$

UnitT	ACQ P83	Serial No
Test EngineerXe	en	
Date17	'/9/10	

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch2	1.99	2.8	140.7mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.99	2.8	140.7mA	>125mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.3	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.3	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.68	2.4	118.8mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.68	2.4	118.8mA	>125mA peak	

Unit	T ACQ	P83	.Serial No
Test Engineer	.Xen		
Date	16/9/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.0	-153.0	22.4	$\checkmark$
Ch2	-143.5	-91.2	-151.2	27.5	$\checkmark$
Ch3	-143.5	-92.8	-152.8	22.9	$\checkmark$
Ch4	-143.5	-92.5	-152.5	23.7	$\checkmark$

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ83P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\checkmark$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ83P
Driver board ID	TACQ83P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	MON249
Monitor board Drawing No/Issue No	D070480_5_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$ 

# LIGO Laboratory / LIGO Scientific Collaboration

LIGO- T0900xxxx

Advanced LIGO UK

March 2010

# Triple Acquisition Driver Unit Test Report

R. M. Cutler, University of Birmingham

Distribution of this document: Inform aligo\_sus

This is an internal working note of the Advanced LIGO Project, prepared by members of the UK team.

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http://www.ligo.caltech.edu/

http://www.physics.gla.ac.uk/igr/sus/

<u>http://www.sr.bham.ac.uk/research/gravity/rh,d,2.html</u> <u>http://www.eng-external.rl.ac.uk/advligo/papers\_public/ALUK\_Homepage.htm</u>

## TRIPLE ACQUISITION DRIVER UNIT BOARD TEST REPORT

Drive Card ID.....T\_ACQ85..... Monitor Card ID....Mon182....

## Contents

- 1 Description
- 2 Test Equipment
- 3 Inspection
- 4 Continuity Checks
- 5 Test Set Up
- 6 Power
- 7 Relay operation
- 8 Monitor Outputs
- 8.1 Amplifier Monitors
- 8.2 Coil Monitors
- 8.3 R.M.S Monitors
- 8.4 Noise Monitors
- 9. Distortion
- 10 Load Tests
- 10.1 Noisy Mode
- 10.2 Low noise Mode
- 10.3 Acquisition Mode
- 11 Noise Measurements
- 12 Final Assembly Tests

## **1. Description**

## **Block diagram**



## Description

The Acquisition unit consists of four identical channels and the power regulators which provide regulated power to the four channels. Each channel consists of a coil drive channel, and monitor circuitry.

The driver has 3 main modes of operation, selectable by two external relay commands: Noisy Mode, Quiet Mode and Acquisition Mode. There is also a mode which switches the channel off.

Unit......T\_ACQ\_P85.....Serial No..... Test Engineer....Xen..... Date......13/10/10.....

## 2. Test equipment

Power supplies (At least +/- 20v variable, 1A) Signal generator (capable of delivering 10v peak, 0.1Hz to 10 kHz) Analogue oscilloscope Agilent Dynamic Signal Analyser (or similar) Low noise Balanced Driver circuit Relay test box

Record the Models and serial numbers of the test equipment used below.

Unit (e.g. DVM)	Manufacturer	Model	Serial Number
Signal Generator	Agilent	33250A	
Oscilloscope	ISO-TECH	ISR622	
PSU*2	Farnell	L30-2	
DVM	Fluke	77	
Signal analyzer	Agilent	35670A	
Pre-amplifier	Stanford Systems	SR560	

## **3. Inspection**

## Workmanship

Inspect the general workmanship standard and comment:  $\sqrt{}$ 

Capacitors C35 and C27 have been changed to 1nF on all channels.

Links: Check that the links W2 and W4 are present on each channel.

Unit	T ACQ P85.	Serial No
Test Engine	er <mark>Xe</mark> n	

Date.....12/10/10.....

## **4. Continuity Checks** Continuity to the V, I and R.M.S Monitor (J1)

### PD out to AA

PIN	SIGNAL	DESCRIPTION	To J1 PIN	OK?
1	PD1P	Photodiode A+	1	$\checkmark$
2	PD2P	Photodiode B+	2	$\checkmark$
3	PD3P	Photodiode C+	3	$\checkmark$
4	PD4P	Photodiode D+	4	$\checkmark$
5	0V	$\checkmark$		
6	PD1N	Photodiode A-	14	$\checkmark$
7	PD2N	Photodiode B-	15	$\checkmark$
8	PD3N	Photodiode C-	16	$\checkmark$
9	PD4N	Photodiode D-	17	$\checkmark$

## LED Mon

PIN	SIGNAL		To J1 PIN	OK?
1	Imon1P		5	$\checkmark$
2	Imon2P		6	$\checkmark$
3	Imon3P		7	$\checkmark$
4	Imon4P		8	$\checkmark$
5	0V	$\checkmark$		
6	Imon1N		18	$\checkmark$
7	Imon2N		19	$\checkmark$
8	Imon3N		20	$\checkmark$
9	Imon4N		21	$\checkmark$

## **PD from Sat**

PIN	SIGNAL	DESCRIPTION	OK?
9	V+ (TP1)	+17v Supply	$\checkmark$
10	V+ (TP1)	+17v Supply	$\checkmark$
11	V- (TP2)	-17v Supply	$\checkmark$
12	V- (TP2)	-17v Supply	$\checkmark$
13	0V (TP3)		$\checkmark$
22	0V (TP3)		$\checkmark$
23	0V (TP3)		$\checkmark$
24	0V (TP3)		$\overline{\mathbf{v}}$
25	0V (TP3)		$\overline{\mathbf{v}}$

## 5. TEST SET UP



Note:

(1) Input signal to differential amplifier is generally stated in the tests below. There is therefore an inherent gain of 2 in the system.

(2) Some signal generators will indicate 1vpk/pk when the output is in fact 1v Peak into the high impedance Differential driver used. The test procedure refers to the actual voltage out of the signal generator.

### **Connections:**

Differential signal inputs to the board under test: Drive Input J3 pins 1, 2, 3, 4 = positive input Drive Input J3 pins 6, 7, 8, 9 = negative input Drive Input J3 pin 5 = ground

Power DC IN J1 pin 9, 10 = +16.5v DC IN J1 pin 11,12 = -16.5 DC IN J1 pins 22, 23, 24, 25 = 0v

OutputsCoil Out to Sat (J4)Ch1+ = J4 pin 1Ch2+ = J4 pin 3Ch3+ = J4 pin 5Ch4+ = J4 pin 7

Unit......T\_ACQ\_P85.....Serial No..... Test Engineer....Xen..... Date......12/10/10.....

## 6. Power

Check the polarity of the wiring from the 3 pin power connector to each of the boards. Viewed from the back of the unit:

A1	Left pin	Positive	White wire
A2	Middle pin	RTN	Black wire
A3	Right pin	Negative	Green wire

## If this is correct,

Connect power to the unit Set the supplies to 16.5v Turn on

**Record Power Supply Currents** 

+ 16.5 supply current (mA)	- 16.5 supply current (mA)
500mA	400mA

Check that all power LEDs are illuminated.

LEDs	Plus	Minus
Front Panel	$\checkmark$	$\checkmark$
Rear Panel	$\checkmark$	$\checkmark$

If the supplies are correct, proceed to the next test.

Unit	T ACQ P85	Serial No	
Test Engineer	Xen		
Date	12/10/10		

## 7. Relay Operation

Operate each relay in turn. Observe its operation. LEDs should illuminate when the relays are operated.

## FILTER

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **TEST RELAYS**

Channel	Indi	Indicator	
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

## **ACQUISITION RELAYS**

Channel	Indicator		OK?
	ON	OFF	
Ch1	$\checkmark$	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$	$\checkmark$

Unit	.T ACQ P85	Serial No
Test Engineer	.Xen	
Date	.12/10/10	

## 8. Monitor Outputs

Switch out the filters and set the unit to Acquisition Mode.

With a 20 Ohm dummy load on each channel, apply an input from the signal generator at 1 kHz, and adjust the amplitude until the output is 1v r.m.s as measured between TP4 and TP5.

Measure the Voltage Monitor outputs with respect to 0v for each channel.

## 8.1 Voltage Monitors

Ch.	Output:	V, I and R.M.S	Expected value	Pass/Fail:
		Monitor		Equal? (+/- 0.1v)
1	0.33	3	0.33v	$\checkmark$
2	0.33	6	0.33v	$\checkmark$
3	0.33	9	0.33v	$\checkmark$
4	0.33	12	0.33v	

Adjust the input voltage until the voltage across the load resistor = 1v r.m.s. Record the current monitor output values.

### **8.2 Current Monitors**

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.92	2	1.86v r.m.s	$\checkmark$
2	1.92	5	1.86v r.m.s	$\checkmark$
3	1.92	8	1.86v r.m.s	$\checkmark$
4	1.92	11	1.86v r.m.s	$\checkmark$

## 8.3 R.M.S Monitors

Ch.	Output	V, I and R.M.S Monitor	Expected Value	Pass/Fail: Equal? (+/- 0.1v)
1	1.96	1	1.86v dc	$\checkmark$
2	1.96	4	1.86v dc	$\checkmark$
3	1.94	7	1.86v dc	$\checkmark$
4	1.95	10	1.86v dc	$\checkmark$

## 8.4 Noise Monitors

- Monitor coil inputs to board were grounded for all channels.

Using the Pre-Amplifier with a gain of 10 and Dynamic Signal Analyser, measure the noise monitor outputs in  $\mu V \sqrt{Hz}$  on the noise monitor outputs. Correct for the pre-amplifier gain. 10pA $\sqrt{Hz}$  should give 2.9 $\mu V \sqrt{Hz}$  out.

Ch.	Output (μV√Hz)	÷(Pre-amplifier gain)	Expected Value	Comparison
1		0.91	2.9µV√Hz	$\checkmark$
2		1.51	2.9µV√Hz	$\checkmark$
3		0.93	2.9µV√Hz	$\checkmark$
4		0.86	2.9µV√Hz	$\checkmark$

Unit	T ACQ P85	Serial No
Test Engineer	.Xen	
Date	12/10/10	

## 9. Distortion

Switch the filters out. Increase input voltage to 5v peak, f = 1kHz. Use 20 Ohm loads. Observe the voltage across each load with an oscilloscope in both Acquisition and Non-Acquisition modes.

	Acquisition Mode: Distortion Free?	Non-Acquisition Mode: Distortion Free?
Ch1	$\checkmark$	$\checkmark$
Ch2	$\checkmark$	$\checkmark$
Ch3	$\checkmark$	$\checkmark$
Ch4	$\checkmark$	$\checkmark$

### **10 Load tests and Frequency response check**

Plug in the 20 Ohm 5W loads. Ensure the links W4 are in place.

### **10.1 Noisy Mode**

With the acquisition mode switched out, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch2	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch3	67.5mV	3.4mA	>2.5mA peak	$\checkmark$
Ch4	67.5mV	3.4mA	>2.5mA peak	$\checkmark$

#### 10Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.067	4.7mA	>2.5mA peak	$\checkmark$
Ch2	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch3	0.066	4.7mA	>2.5mA peak	$\checkmark$
Ch4	0.066	4.7mA	>2.5mA peak	$\checkmark$

#### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.326	23.0mA	>2.5mA peak	$\checkmark$
Ch2	0.325	23.0mA	>2.5mA peak	$\checkmark$
Ch3	0.324	22.9mA	>2.5mA peak	$\checkmark$
Ch4	0.321	22.7mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch2	0.391	27.6mA	>2.5mA peak	$\checkmark$
Ch3	0.390	27.6mA	>2.5mA peak	$\checkmark$
Ch4	0.389	27.5mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch2	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch3	0.414	29.3mA	>2.5mA peak	$\checkmark$
Ch4	0.415	29.3mA	>2.5mA peak	$\checkmark$

Unit	T ACQ	P85	.Serial No
Test Engineer	Xen	-	
Date	13/10/10		

## 10.2 Low noise Mode

With the acquisition mode switched out and filters switched in, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter, at the frequencies below. For 1Hz and 10Hz, use the oscilloscope. Calculate the output current in each case (Vout/20).

#### 1Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	45mV	2.3mA	>2.5mA peak	
Ch2	45mV	2.3mA	>2.5mA peak	
Ch3	45mV	2.3mA	>2.5mA peak	
Ch4	45mV	2.3mA	>2.5mA peak	

## 10Hz

	Vo peak	Peak lo (Vo/20)	Specification	Pass/Fail
Ch1	13mV	650uA	>2.5mA peak	
Ch2	16mV	800uA	>2.5mA peak	
Ch3	16mV	800uA	>2.5mA peak	
Ch4	15mV	750uA	>2.5mA peak	

### 100Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.128	9.0mA	>2.5mA peak	$\checkmark$
Ch2	0.132	9.3mA	>2.5mA peak	$\checkmark$
Ch3	0.131	9.3mA	>2.5mA peak	$\checkmark$
Ch4	0.127	9.0mA	>2.5mA peak	$\checkmark$

### 200Hz

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.244	17.3mA	>2.5mA peak	$\checkmark$
Ch2	0.249	17.6mA	>2.5mA peak	$\checkmark$
Ch3	0.248	17.5mA	>2.5mA peak	$\checkmark$
Ch4	0.243	17.2mA	>2.5mA peak	$\checkmark$

	Vo r.m.s	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch2	0.371	26.2mA	>2.5mA peak	$\checkmark$
Ch3	0.370	26.2mA	>2.5mA peak	$\checkmark$
Ch4	0.369	26.1mA	>2.5mA peak	$\checkmark$

UnitT	ACQ	P85	.Serial No
Test EngineerX	en		
Date13	3/10/10		

### **10.3 Acquisition Mode**

With the acquisition mode switched in, and filters switched out, apply 5v peak at the input to the drive unit. Measure the r.m.s differential voltage across each load resistor in turn using a true r.m.s meter at the frequencies below. Calculate the peak voltages, then the peak output current in each case (Vout/20).

### 100Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.97	2.8	139.3mA	>125mA peak	$\checkmark$
Ch2	1.96	2.8	138.6mA	>125mA peak	$\checkmark$
Ch3	1.98	2.8	140.0mA	>125mA peak	$\checkmark$
Ch4	1.97	2.8	139.3mA	>125mA peak	$\checkmark$

## 200Hz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch2	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch3	2.2	3.1	155.5mA	>125mA peak	$\checkmark$
Ch4	2.2	3.1	155.5mA	>125mA peak	$\checkmark$

#### 1 kHz

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch2	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch3	2.3	3.1	162.6mA	>125mA peak	$\checkmark$
Ch4	2.3	3.1	162.6mA	>125mA peak	$\checkmark$

	Vo r.m.s	Vo pk.	Peak lo (Vo/20) x 1.414	Specification	Pass/Fail
Ch1	1.67	2.4	118.1mA	>125mA peak	
Ch2	1.67	2.4	118.1mA	>125mA peak	
Ch3	1.67	2.4	118.1mA	>125mA peak	
Ch4	1.67	2.4	118.1mA	>125mA peak	

Unit	.T_ACQ_P	85	Serial No
Test Engineer	.Xen		
Date	.13/10/10		

## **11. Noise Measurements**

As the previous test involves non – representative temperature rises, allow the unit to cool before performing this test.

Replace the filter links W4, on each channel.

Connect the filter test box, and switch in all filters.

Switch it out of Test Mode and out of the Acquisition mode

Use the HP 35670A Dynamic Signal Analyser.

Connect a shorting plug to the demand input to short all positive and negative demands together and to 0v. Connect 20 Ohm loads to the outputs.

Use Stuart Aston's noise measurement set up, loaded from disc.

Measure the noise output from each channel in turn at the amplifier outputs (TP4 and TP5). The Low Pass filter on the SR650 may be used to reduce mains interference, to prevent the Signal Analyser from overloading. Ideally the filter corner frequency should be set to 3 kHz. Set the amplifier gain to 1000, and check that the overload light is not on before each measurement.



### Measure the noise output at 10 Hz.

	Spec in dB V√Hz	Measured @ 10Hz	- 60dB =	Measured in nV√Hz	OK?
Ch1	-143.5	-93.3	-153.3	21.6	$\checkmark$
Ch2	-143.5	-87.5	-147.5	42.2	$\checkmark$
Ch3	-143.5	-92.5	-152.5	23.7	$\checkmark$
Ch4	-143.5	-93.1	-153.1	22.1	

## Notes:

Specified noise output current at 10 Hz =  $10pA\sqrt{Hz}$  (worst case) Total resistance at 10Hz, in Low noise mode = 6.7k Amplifier noise voltage should therefore be = 67 nV $\sqrt{Hz}$ 67 nV $\sqrt{Hz}$  = -143.5 dB $\sqrt{Hz}$  Unit.....TACQ85P....Serial No ..... Test Engineer ......RMC Date ......4/11/10

## **12. Final Assembly Tests**

- 1. Remove the lid of the box.  $\sqrt{}$
- 2. Unplug all external connections.  $\sqrt{}$

3. Check that the 4 pillars are in place in the corners of the Boards and that their screws are tight.  $\surd$ 

- 4. Check that all internal connectors are firmly mated.  $\sqrt{}$
- 5. Tighten the screw-locks holding all the external connectors.  $\sqrt{10}$
- 6. Check that all the LEDs are nicely centred.  $\sqrt{}$
- 7. Check that all links W4 are in place.  $\sqrt{}$

8. Check that the boards are labelled with their Drawing Number, Issue Number, and serial number. Record below:

UoB box ID	TACQ85P
Driver board ID	TACQ85P
Driver board Drawing No/Issue No	D0901047_V4
Monitor board ID	M0N182
Monitor board Drawing No/Issue No	D070480_4_K

9. Check the security of any modification wires. None

- 10. Visually inspect.  $\sqrt{}$
- 11. Put the lid on and fasten all screws,  $\sqrt{}$

Check all external screws for tightness.  $\sqrt{}$