

A

B

C

D

A

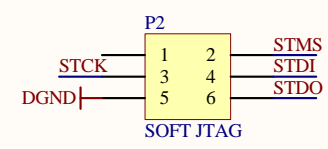
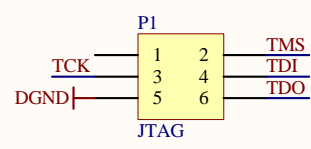
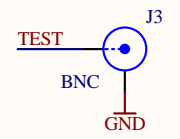
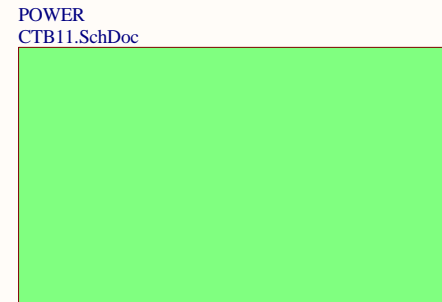
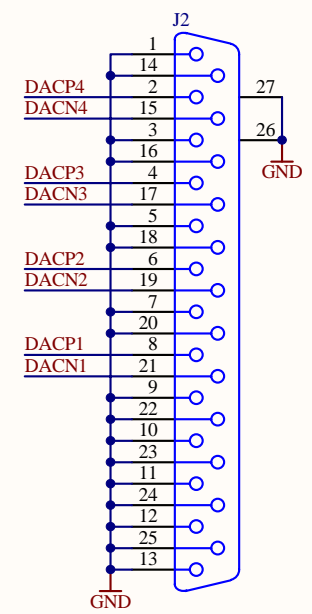
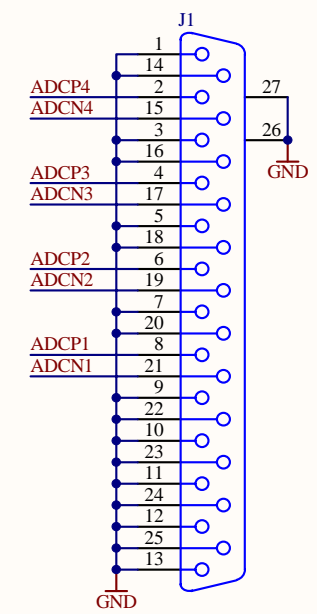
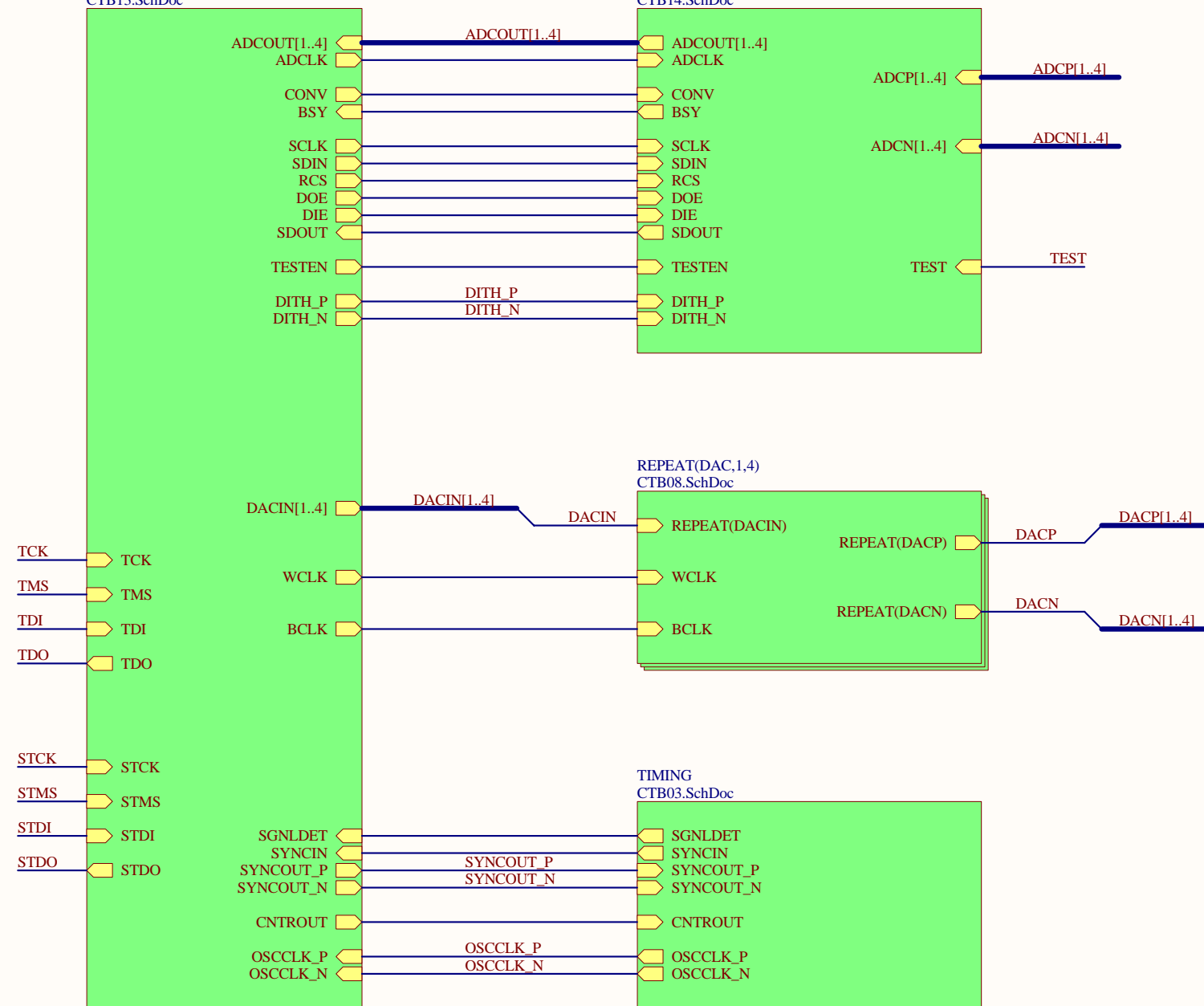
B

C

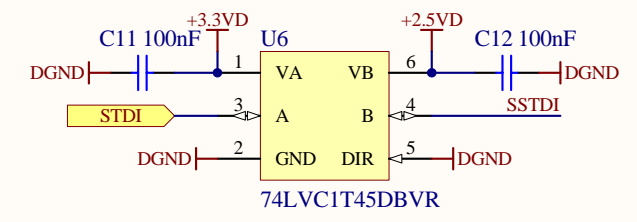
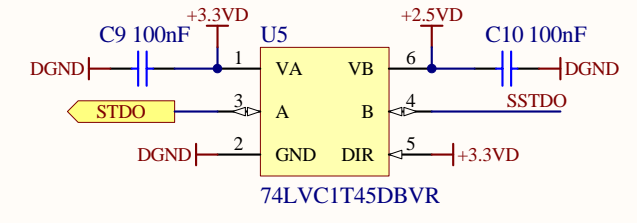
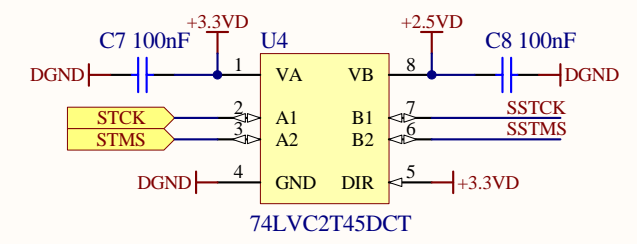
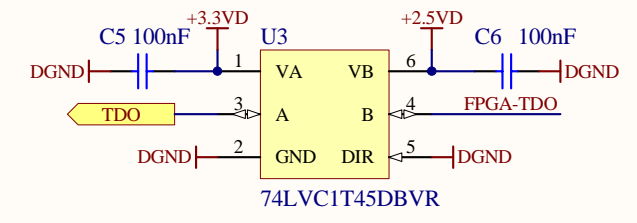
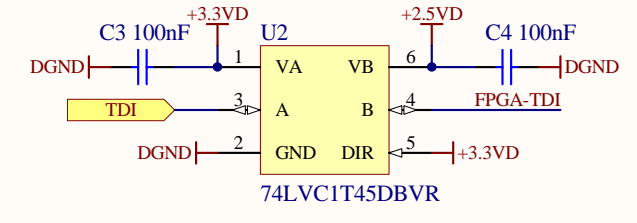
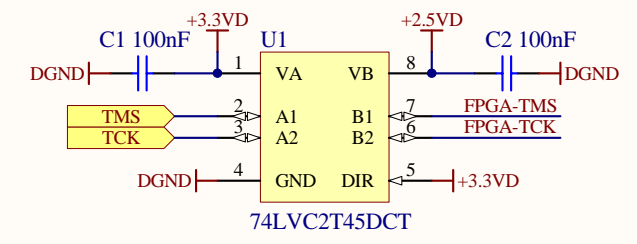
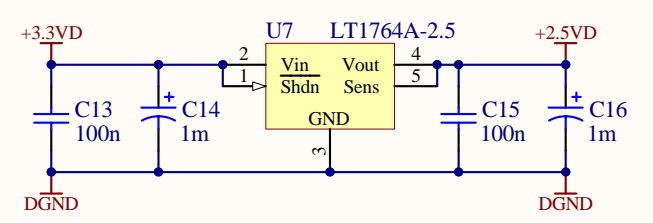
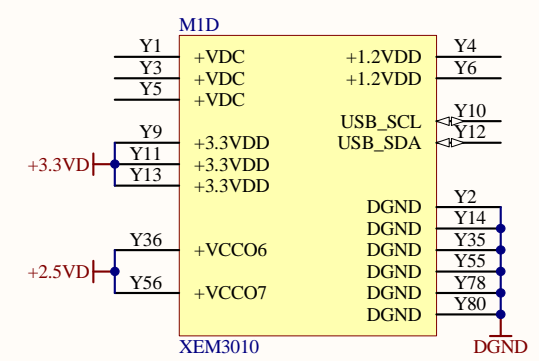
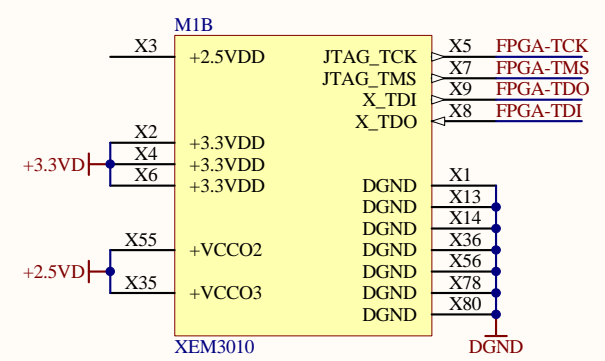
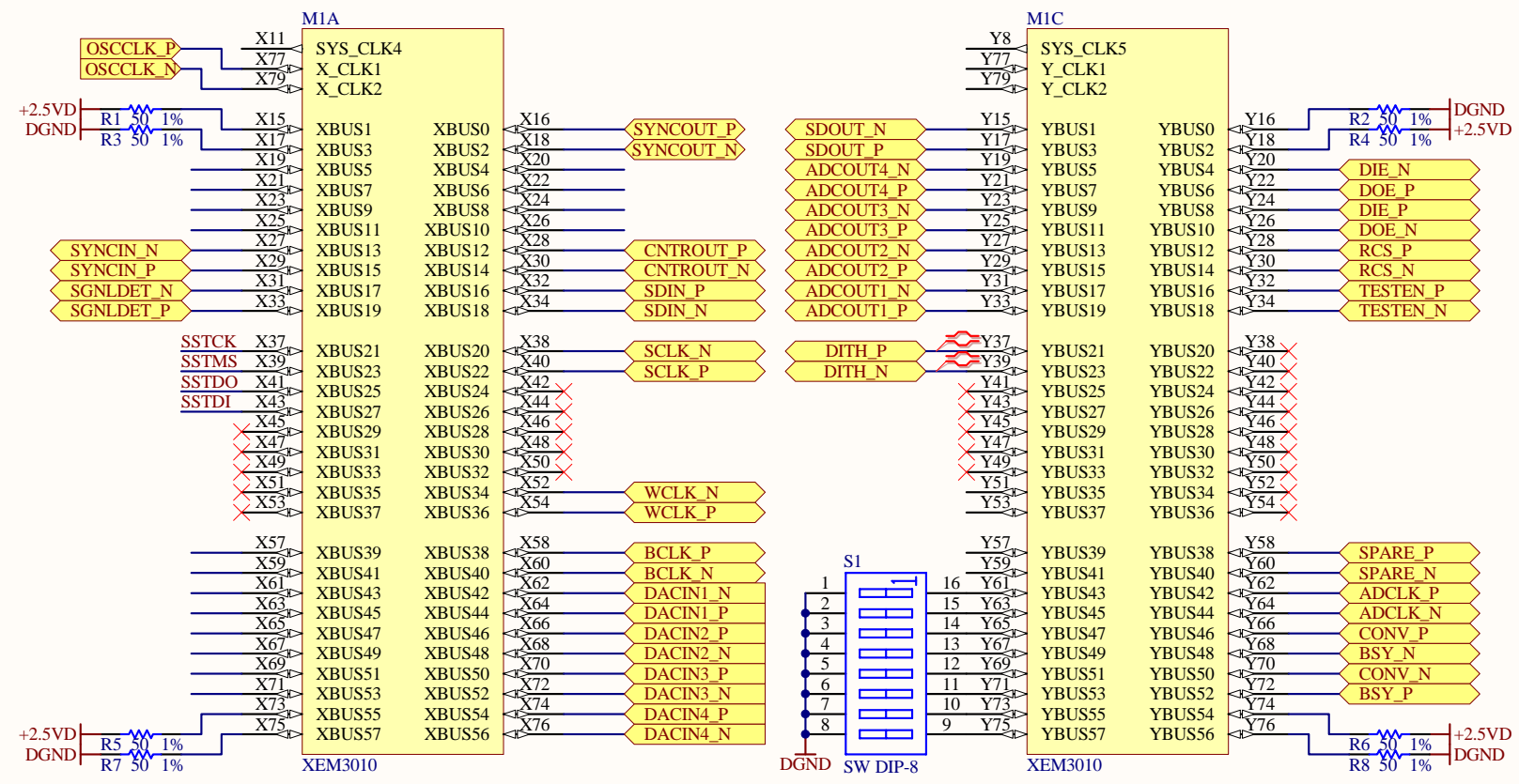
D

FPGA INTERFACE  
CTB13.SchDoc

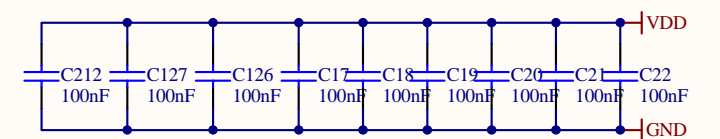
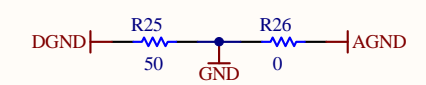
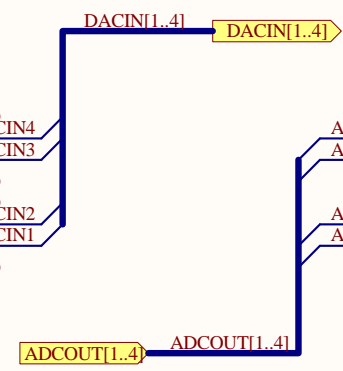
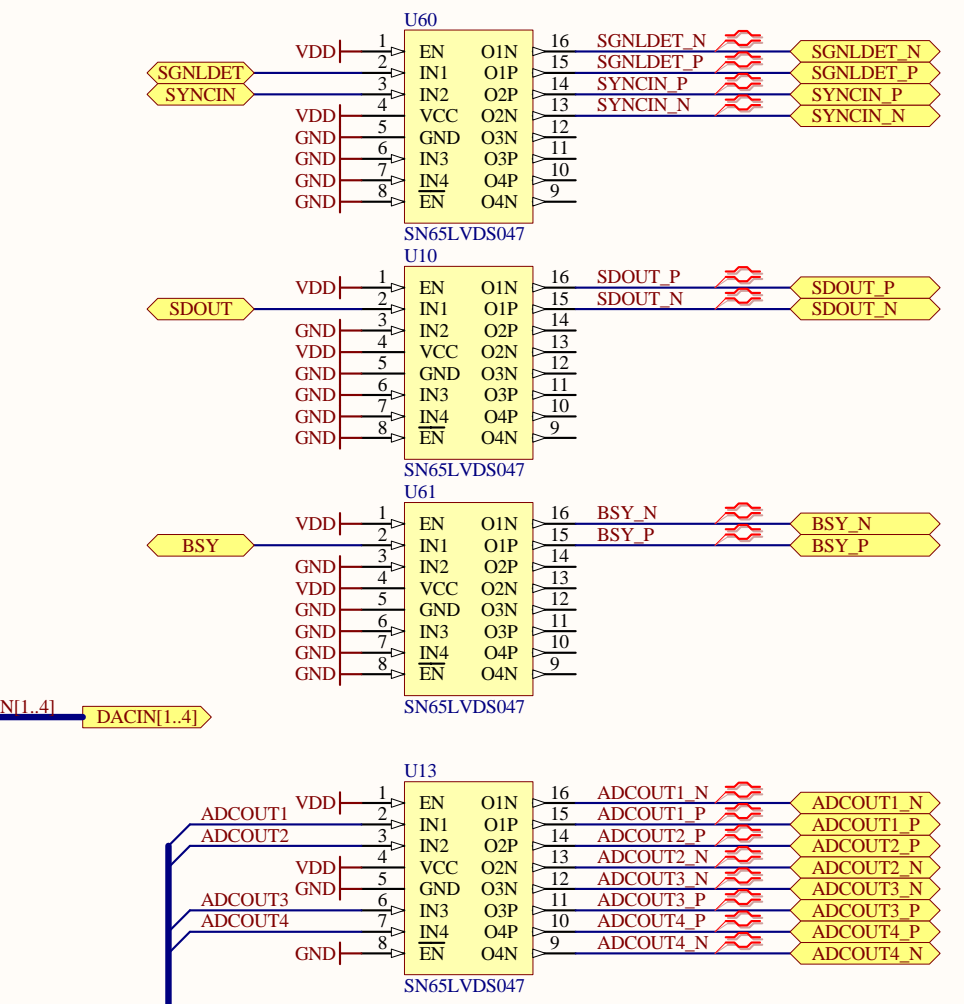
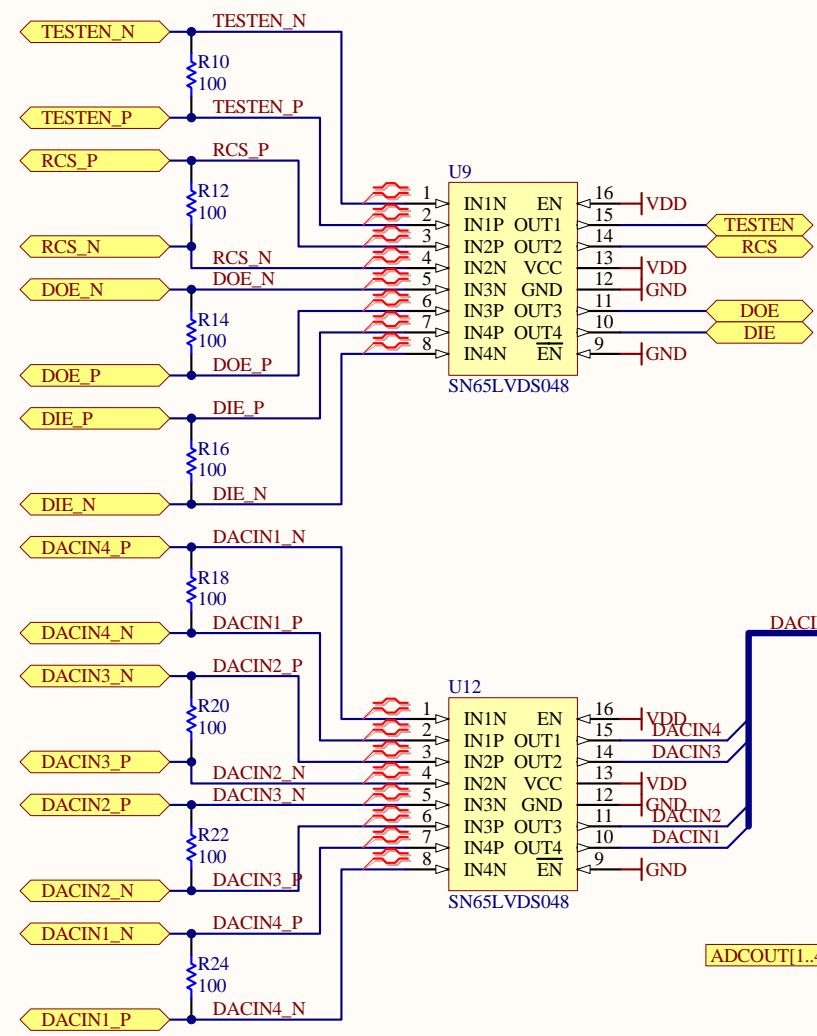
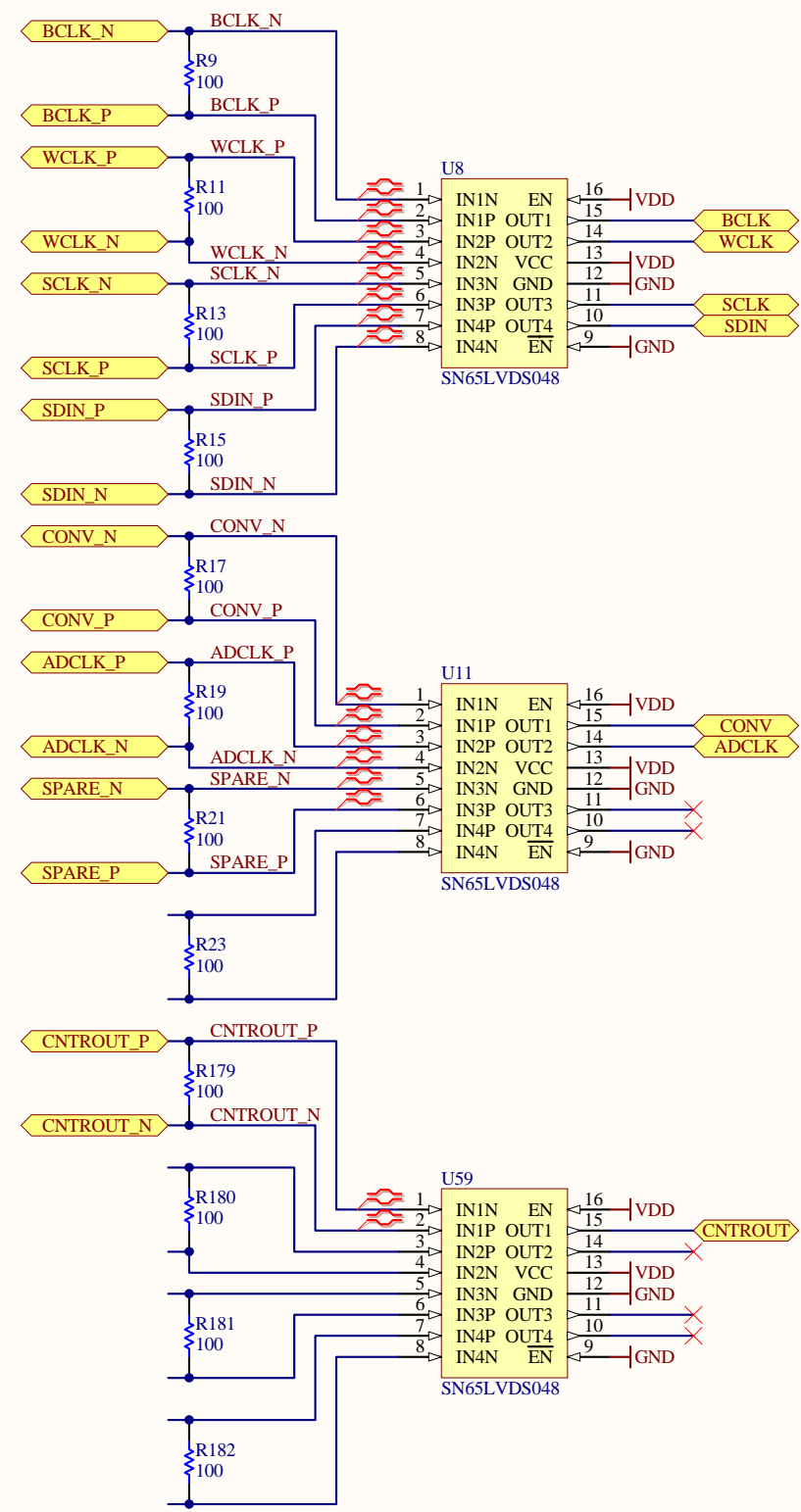
QUADADC  
CTB14.SchDoc



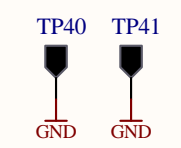
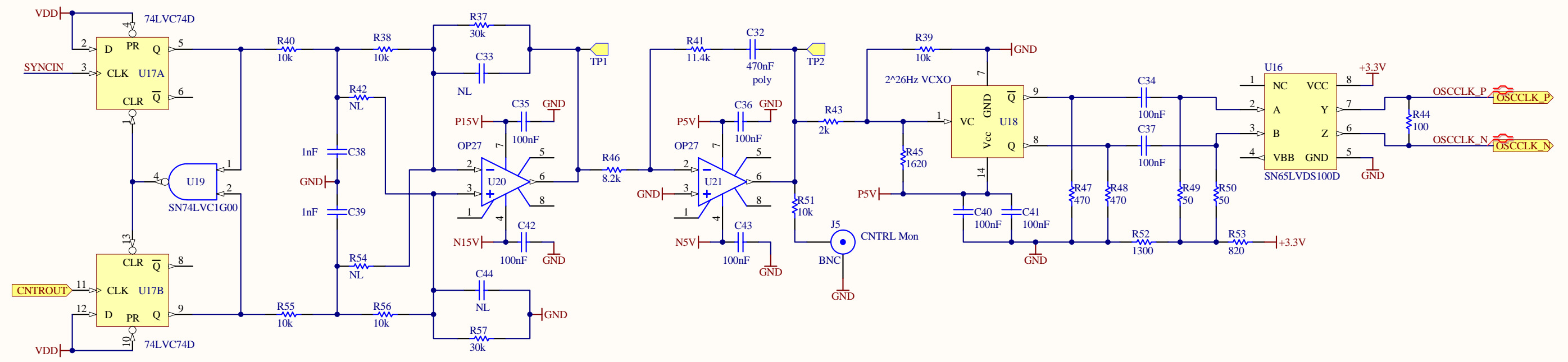
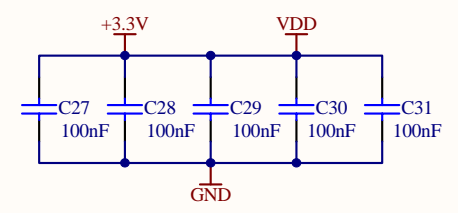
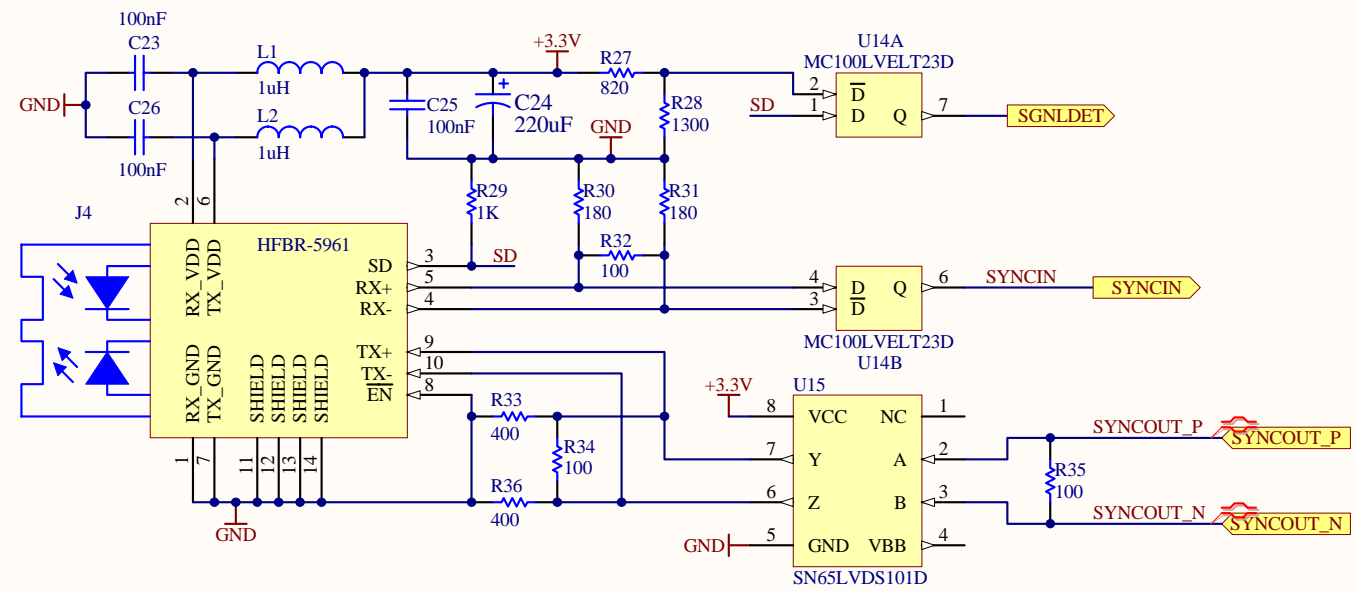
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Size B	Number <b>D060118</b>	Revision <b>A</b>
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File: C:\User\...\CTB00.SchDoc	Drawn By: <b>Paul Schwinberg</b>	



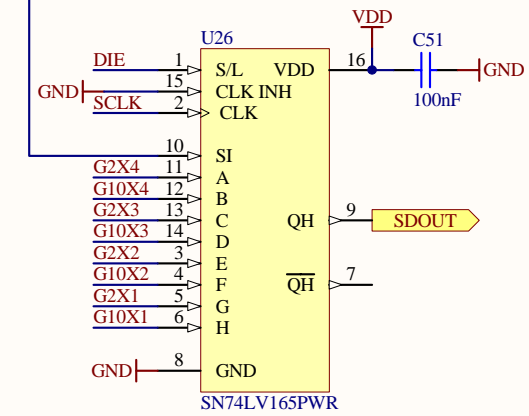
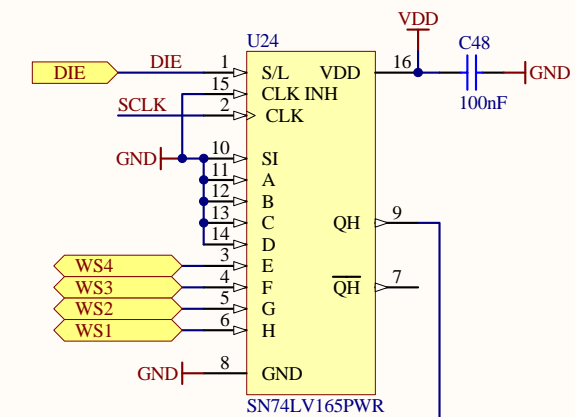
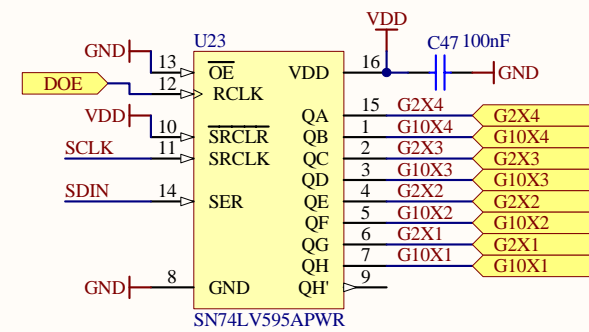
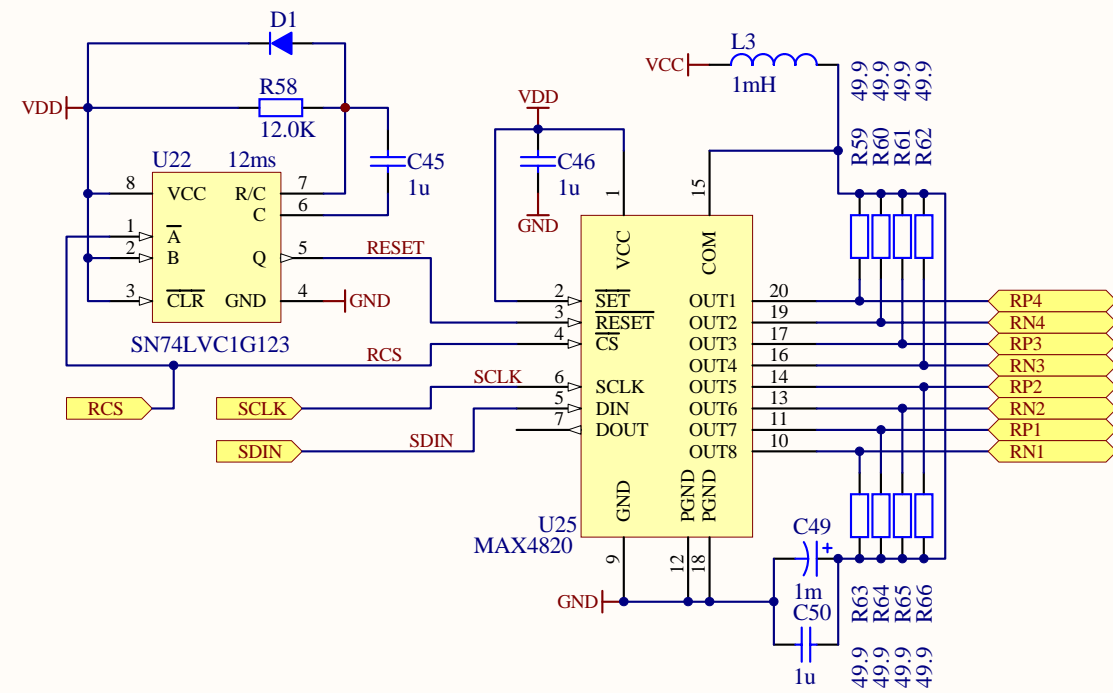
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Size B	Number <b>D060118</b>	Revision <b>A</b>
Date: 6/19/2007	Sheet of	
File: C:\User\...\CTB01.SchDoc	Drawn By: Paul Schwinberg	



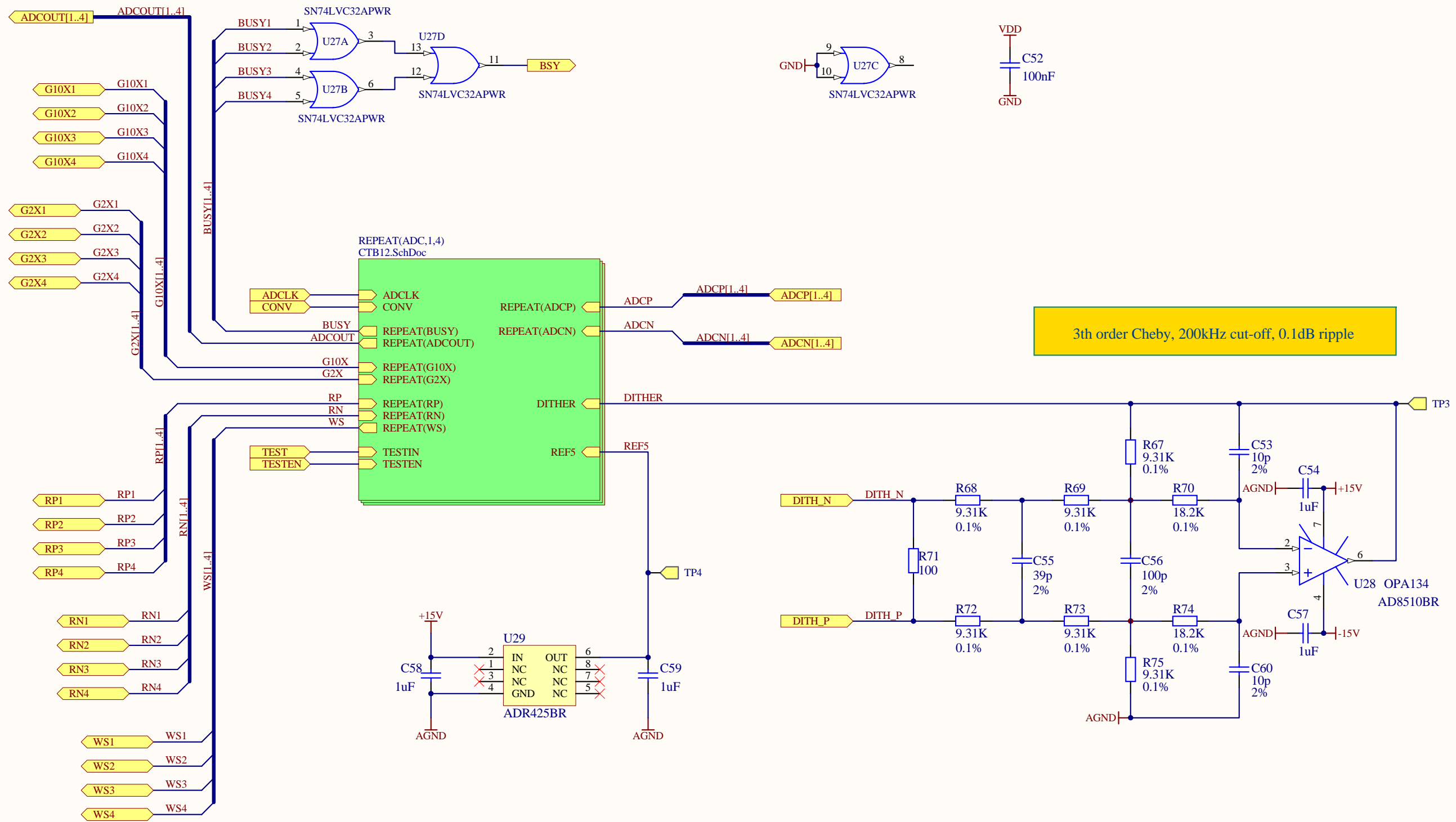
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Size B	Number <b>D060118</b>	Revision <b>A</b>
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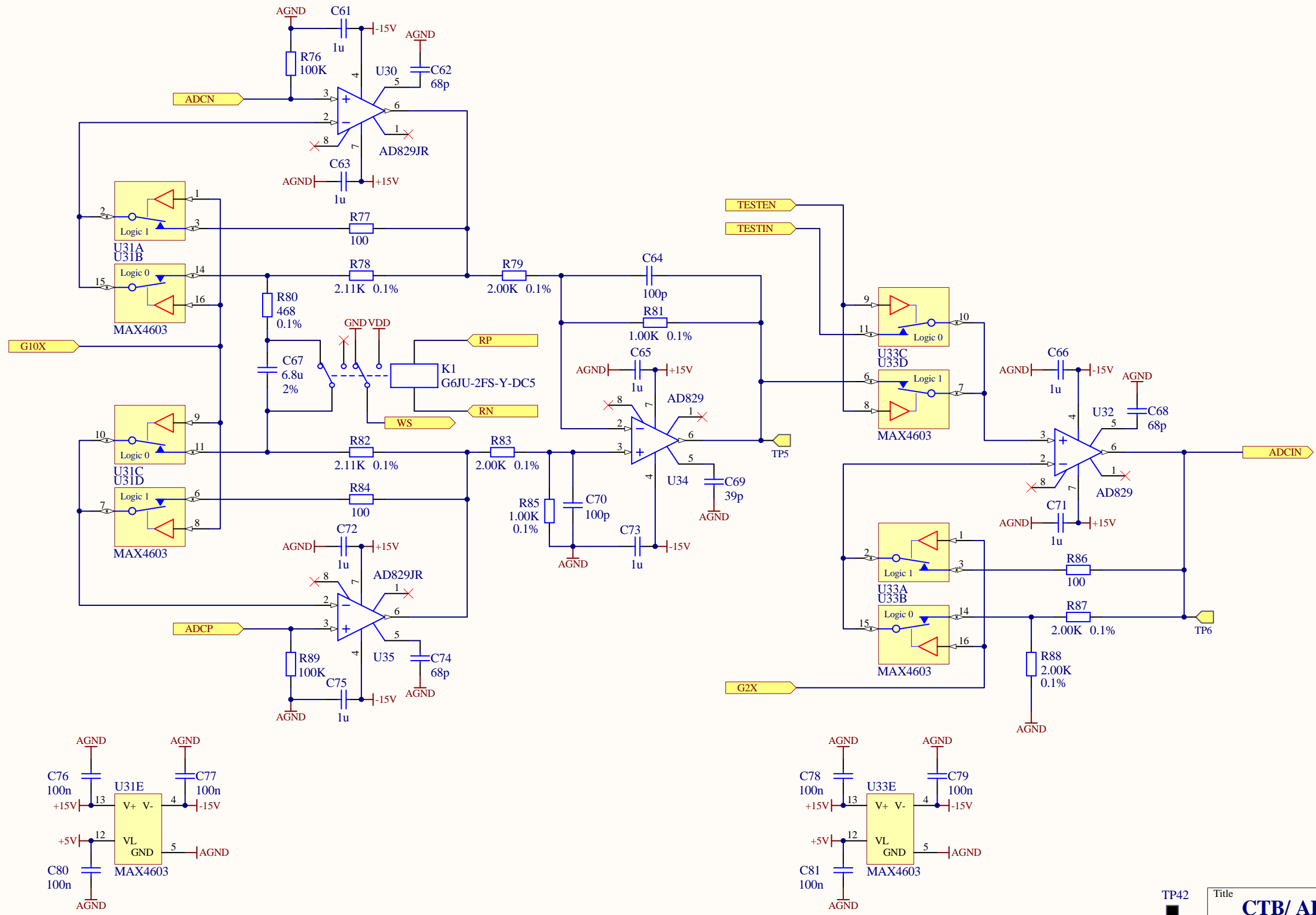
Title		
<b>CTB/ Oscillator Locking</b>		
Size	Number	Revision
B	D060118	A
Date:	6/19/2007	Sheet 2 of 4
File:	C:\User\...\CTB03.SchDoc	Drawn By: Paul Schwinberg



Title		
<b>CTB/ ADC Front End Control</b>		
Size	Number	Revision
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Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB04.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg

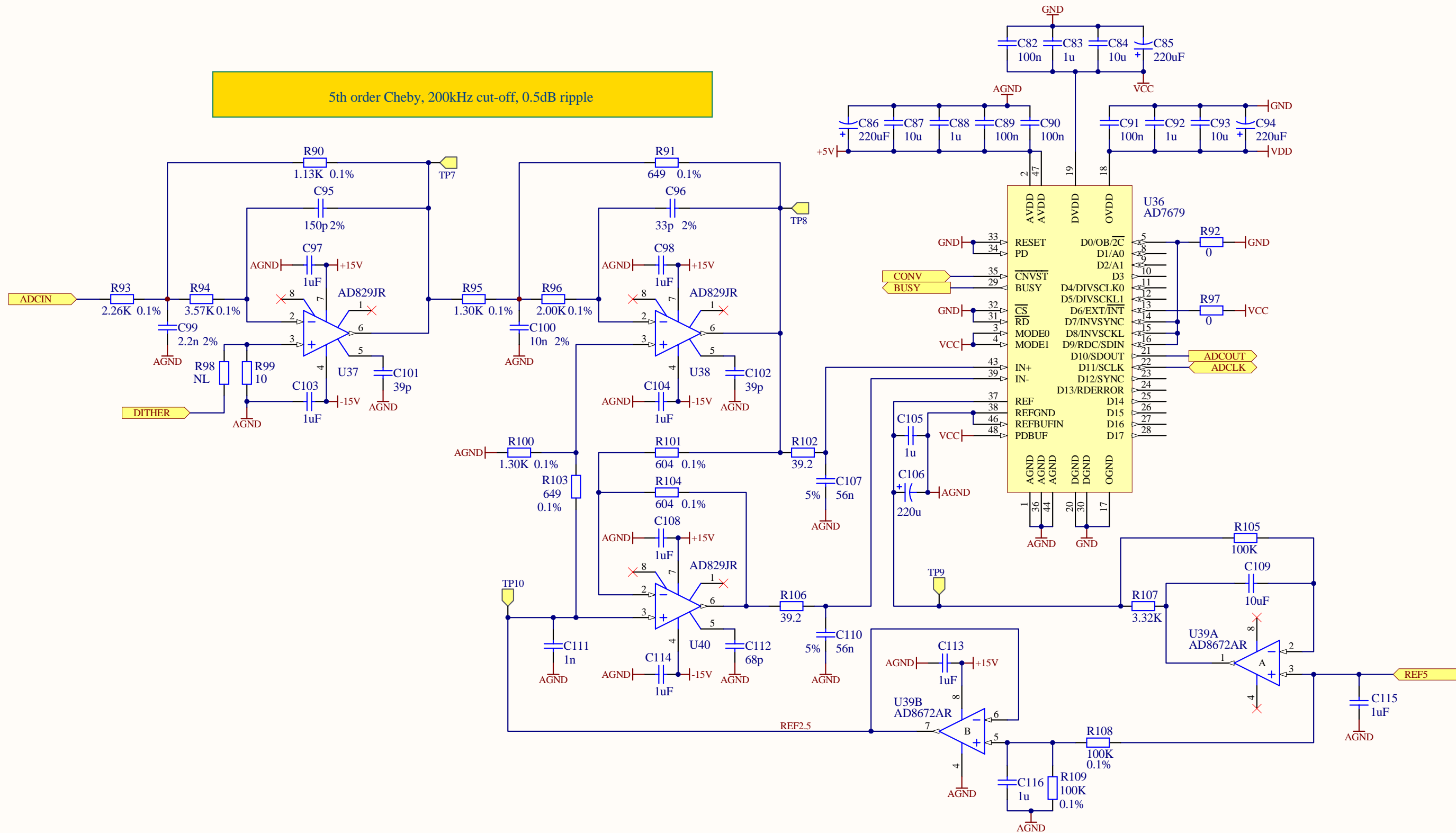


Title		
<b>CTB/ 4 Channel ADC</b>		
Size	Number	Revision
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Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB05.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg



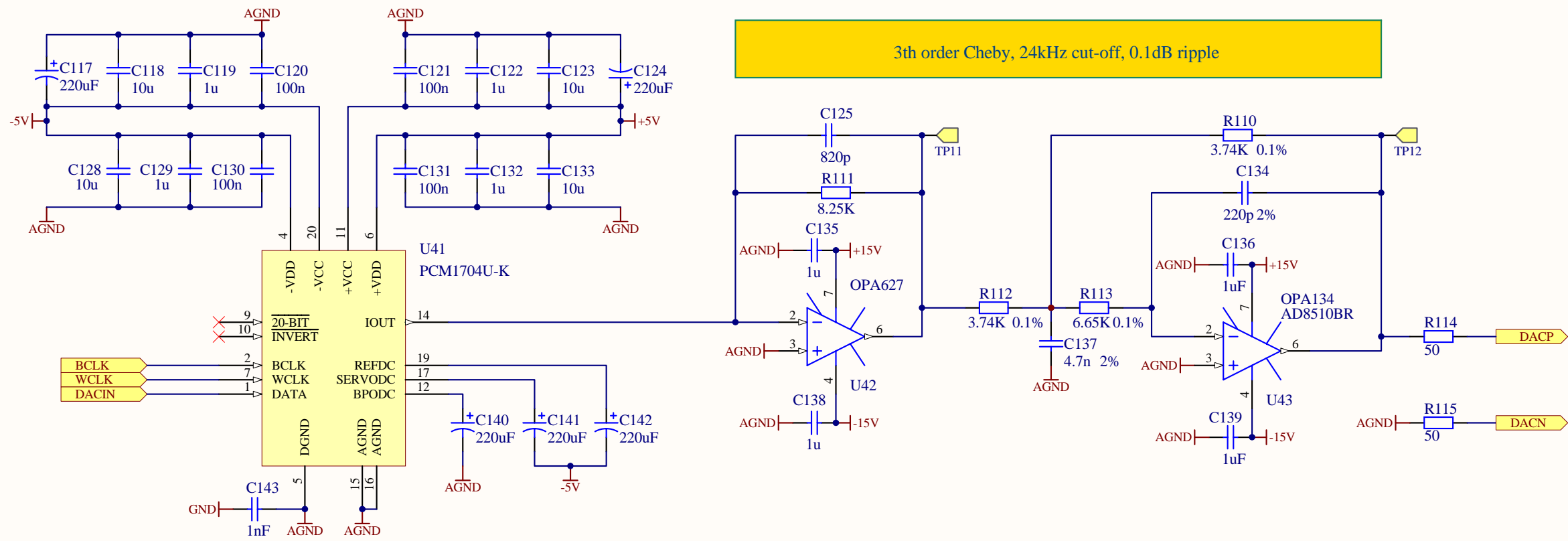
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Size B	Number <b>D060118</b>	Revision <b>A</b>
Date: 6/19/2007	Sheet 6 of 11	
File: C:\User\...\CTB06.SchDoc	Drawn By: Daniel Sigg	



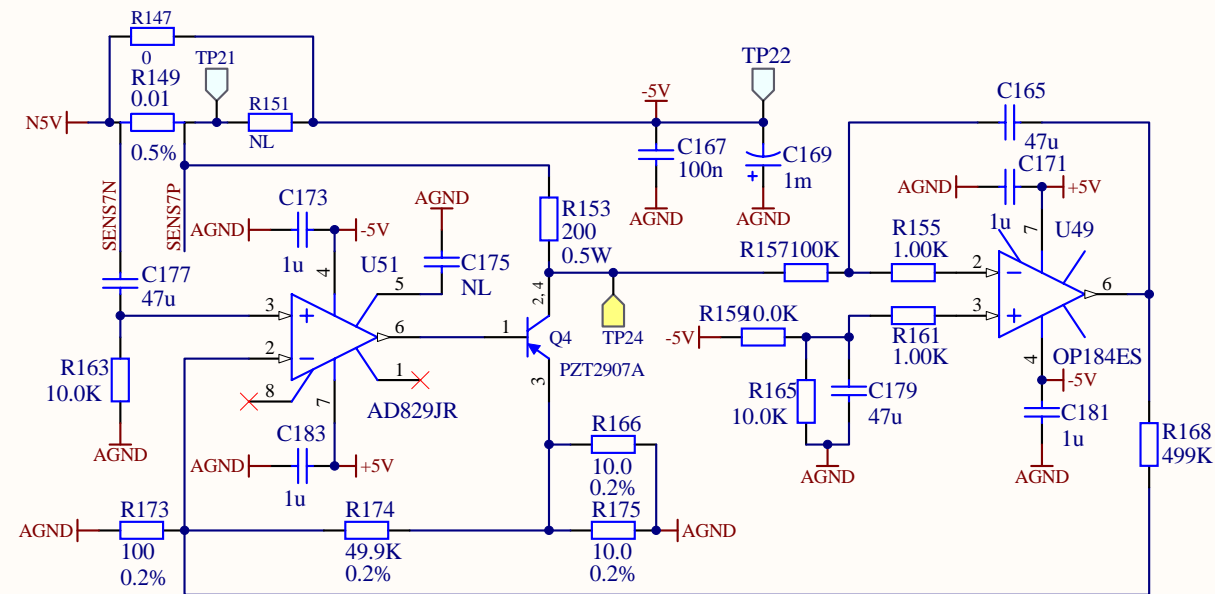
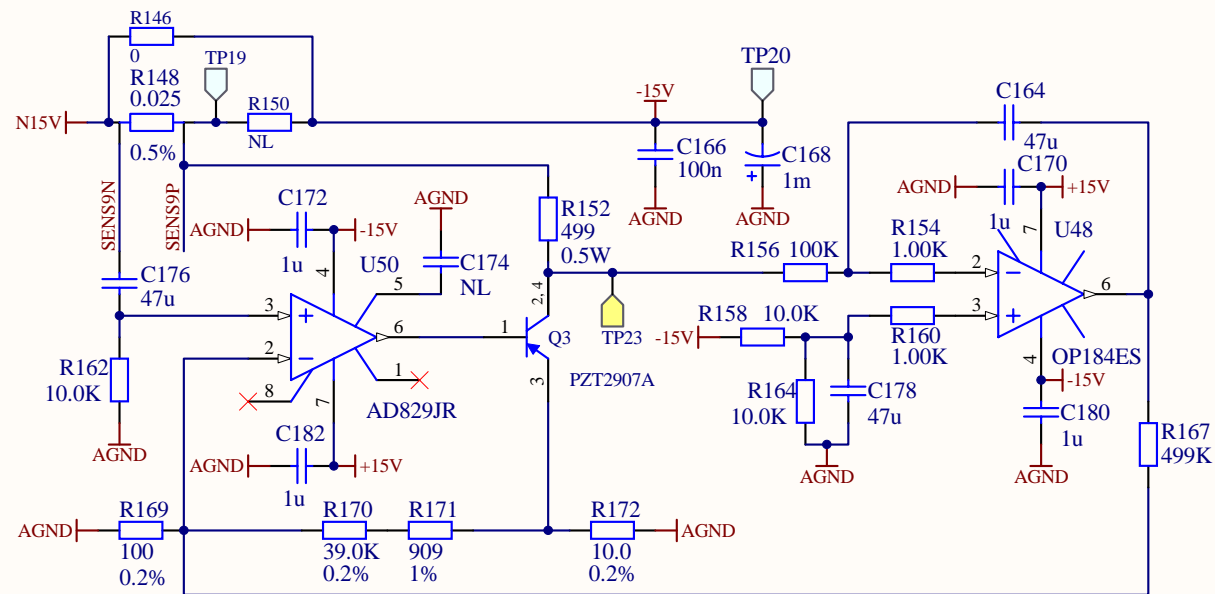
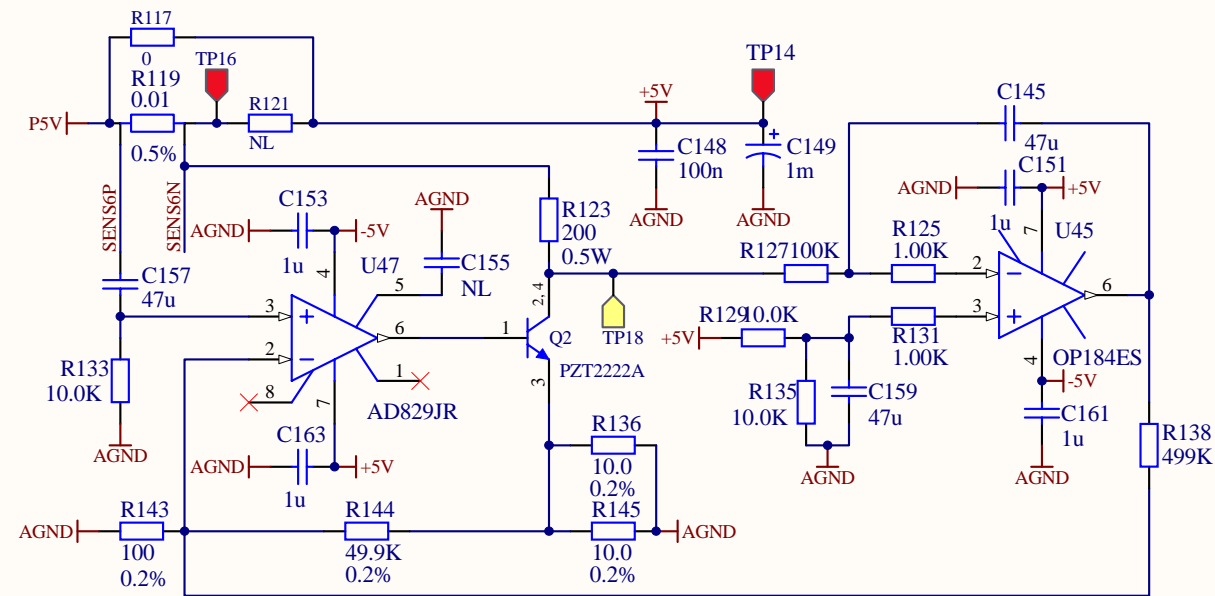
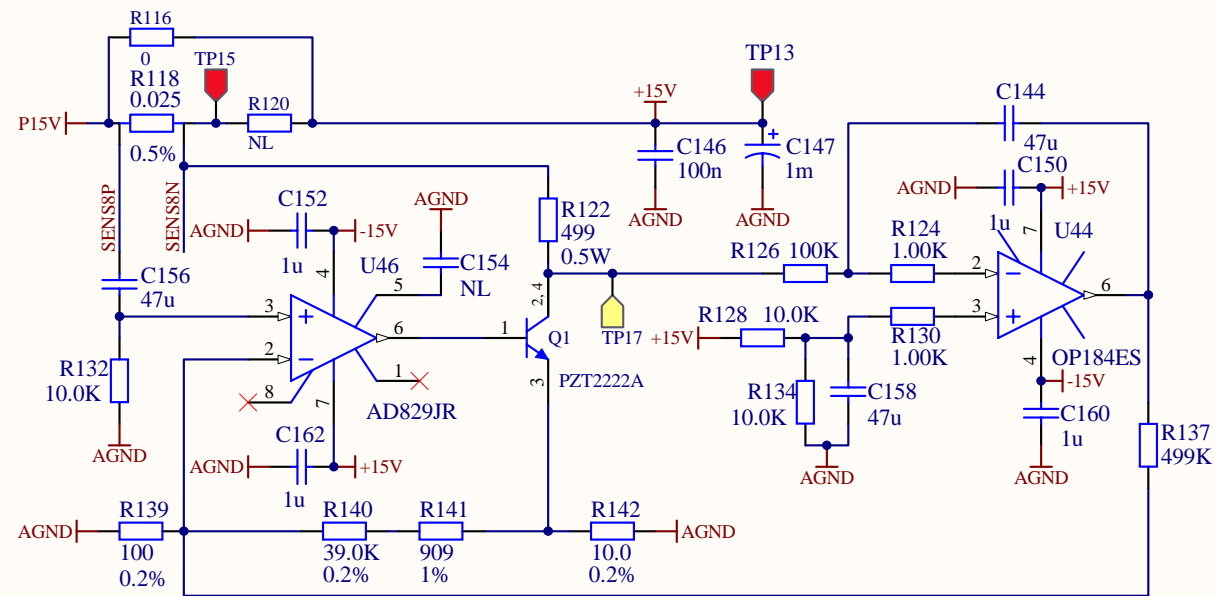


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<b>CTB/ ADC Main</b>		
Size	Number	Revision
B	<b>D060118</b>	<b>A</b>
Date:	6/19/2007	Sheet 7 of 11
File:	C:\User\...\CTB07.SchDoc	Drawn By: Daniel Sigg/ Paul Schwinberg

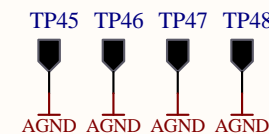




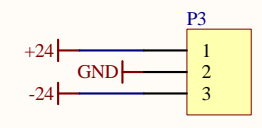
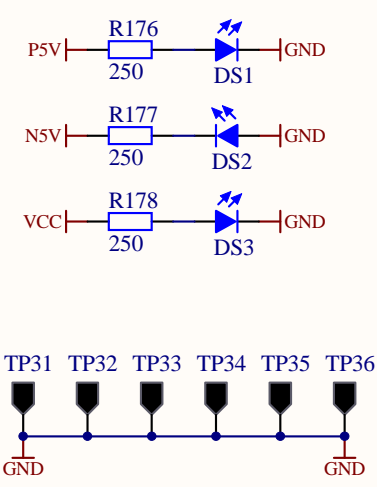
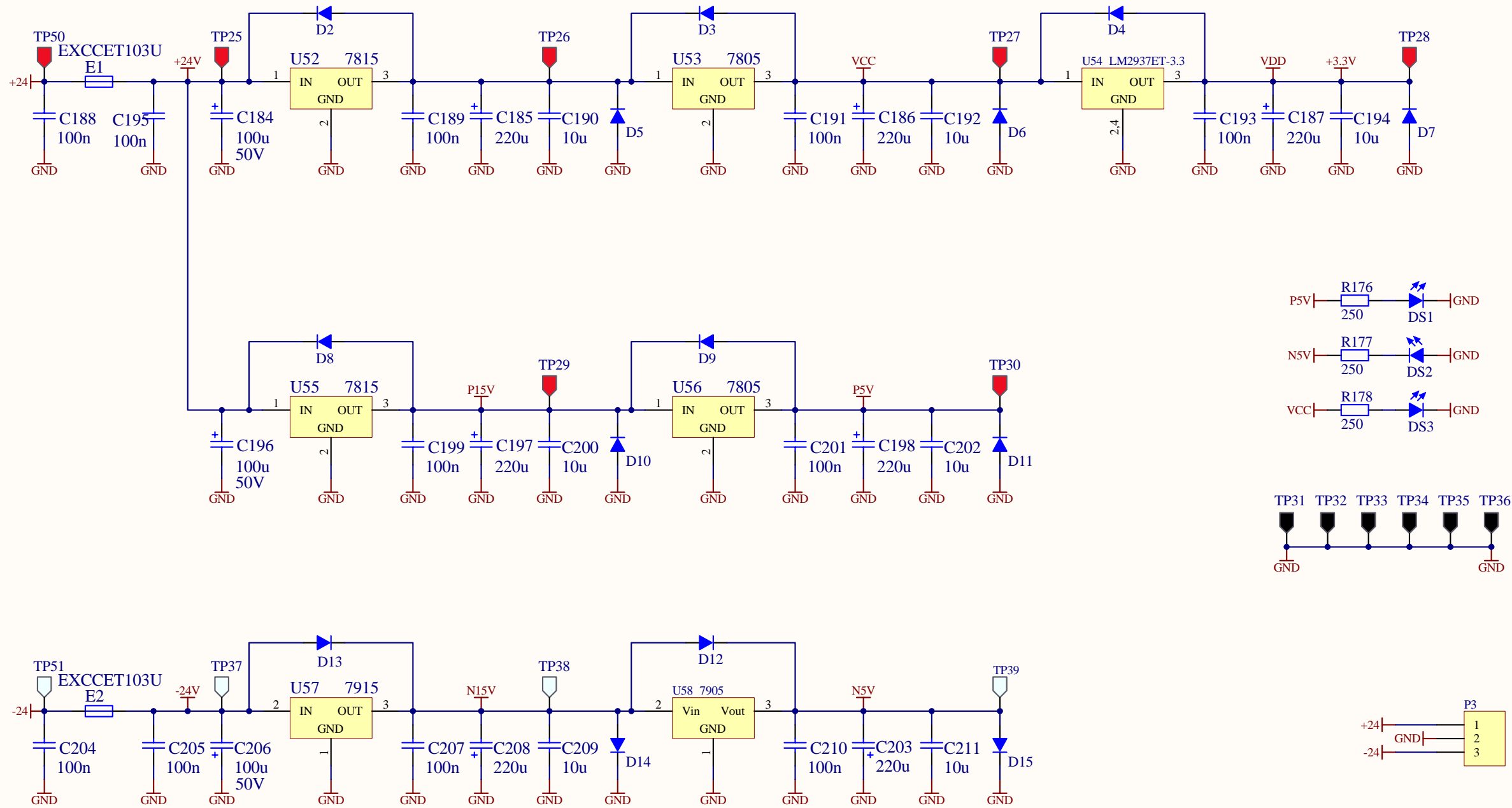
Title <b>CTB/ DAC</b>		
Size B	Number <b>D060118</b>	Revision <b>A</b>
Date: 6/19/2007	Sheet 9 of 11	
File: C:\User\...\CTB08.SchDoc	Drawn By: Daniel Sigg/ Paul Schwinberg	



noise eater/current shunt: 40dB min. suppression, +/-100uV max. range



Title		
<b>CTB/ Power Noise Eaters</b>		
Size	Number	Revision
B	D060118	A
Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB09.SchDoc	Drawn By Daniel Sigg/ Paul Schwinberg



Title		
<b>CTB/ Power Regulators</b>		
Size	Number	Revision
B	D060118	A
Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB10.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg

1

2

3

4

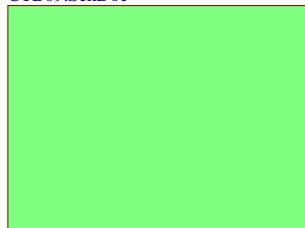
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6

A

A

Power Noise Eaters  
CTB09.SchDoc



Voltage Regulators  
CTB10.SchDoc



B

B

C

C

D

D

Title		
<b>CTB/ Power</b>		
Size	Number	Revision
B	<b>D060118</b>	<b>A</b>
Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB11.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg

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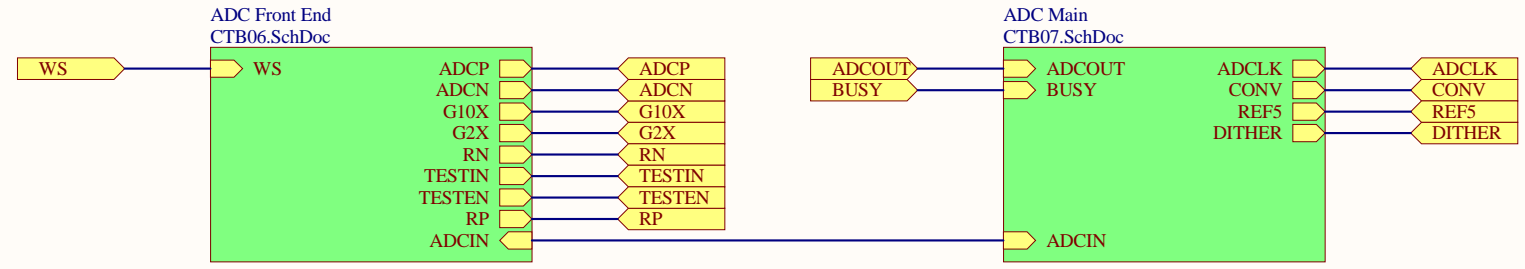
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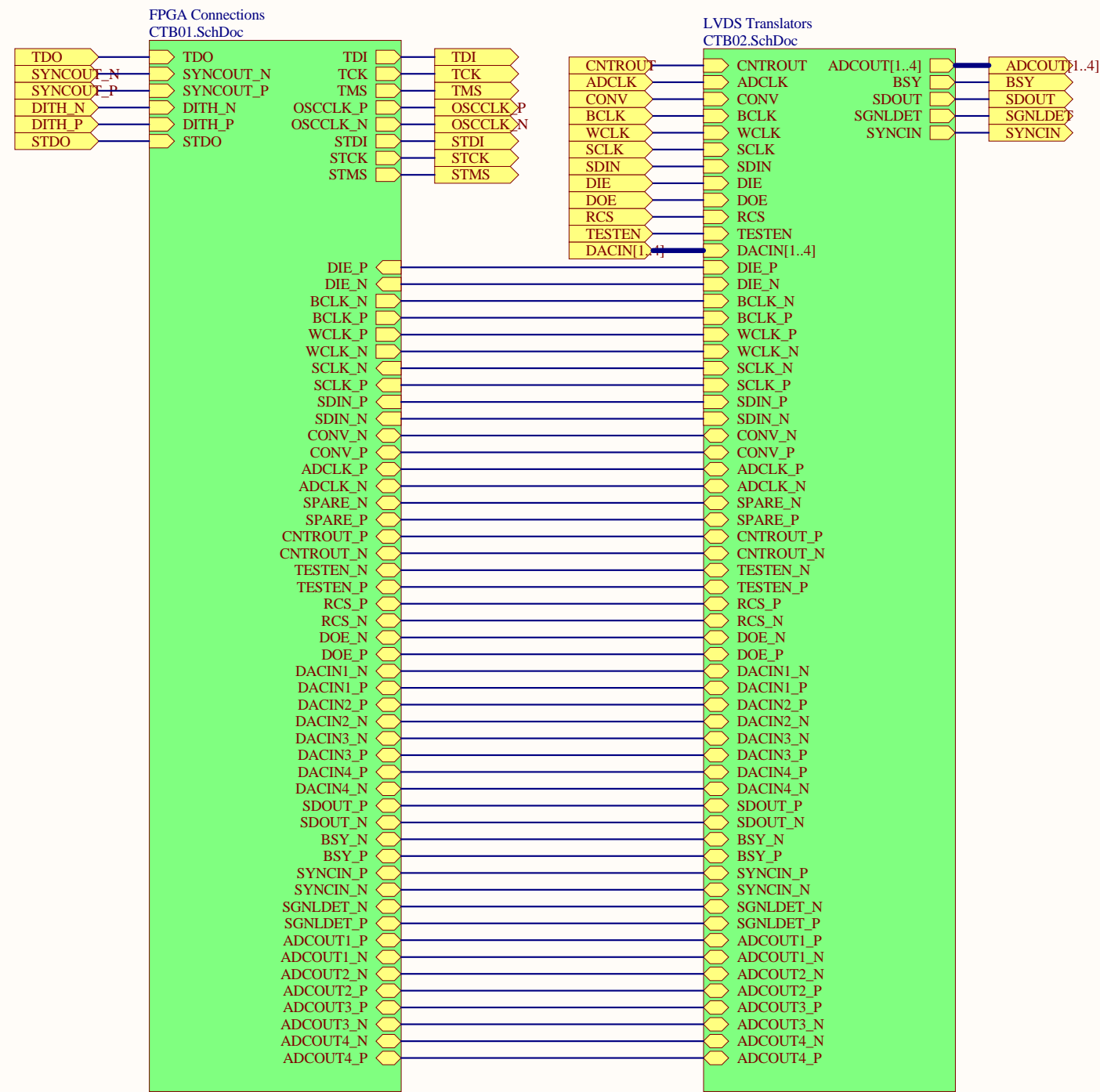
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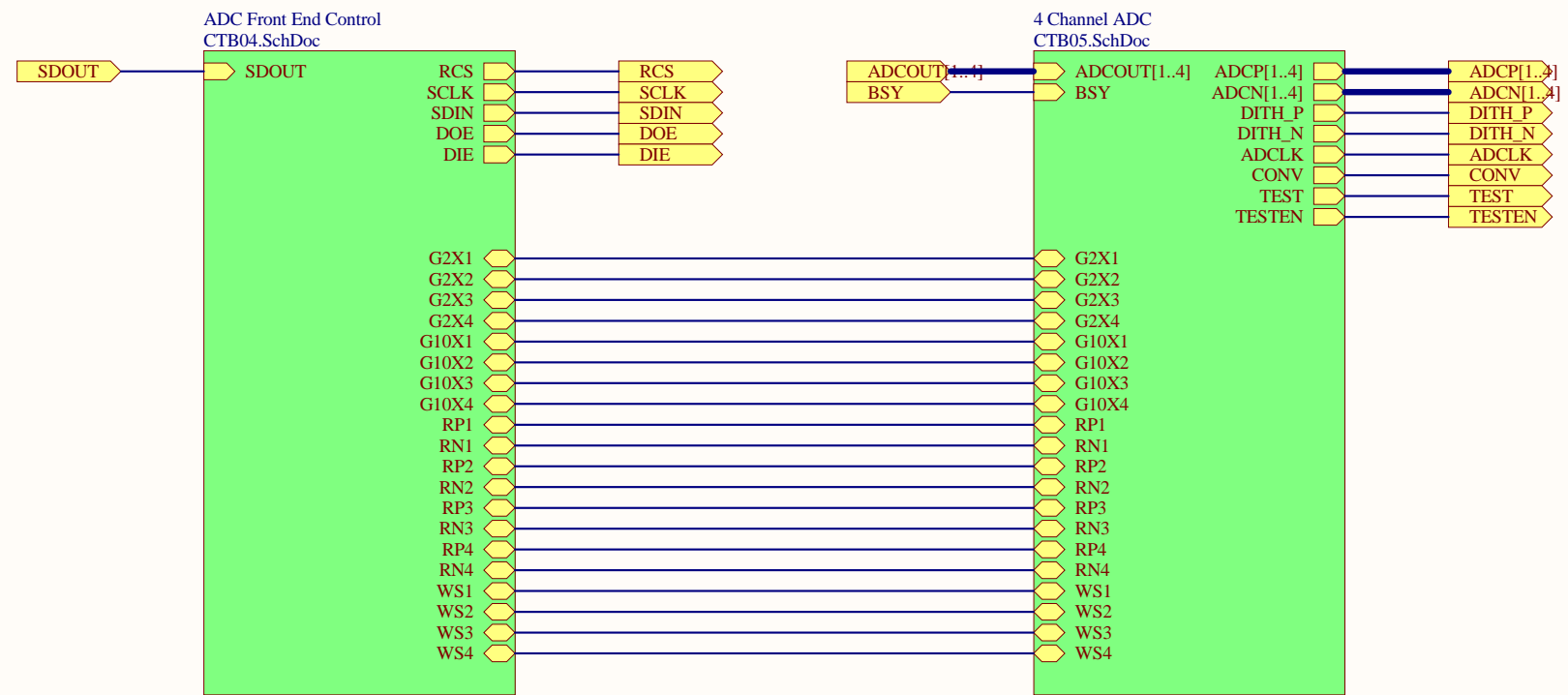
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Title		
<b>CTB/ ADC</b>		
Size	Number	Revision
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Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB12.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg



Title		
<b>CTB/ FPGA Interface</b>		
Size	Number	Revision
B	D060118	A
Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB13.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg



Title		
<b>CTB/ Quad ADC</b>		
Size	Number	Revision
B	<b>D060118</b>	<b>A</b>
Date:	6/19/2007	Sheet of
File:	C:\User\...\CTB14.SchDoc	Drawn By: Paul Schwinberg/ Daniel Sigg