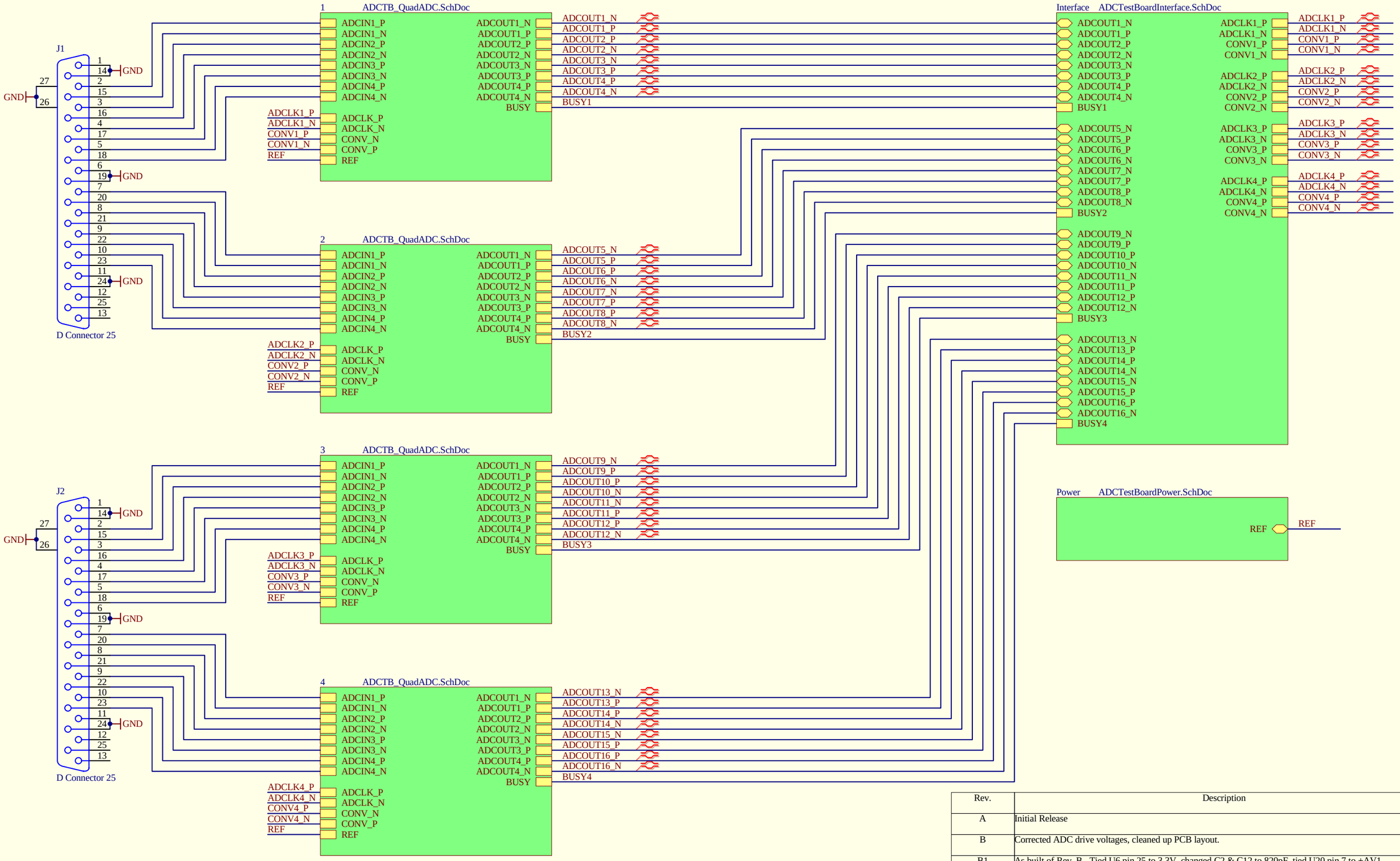
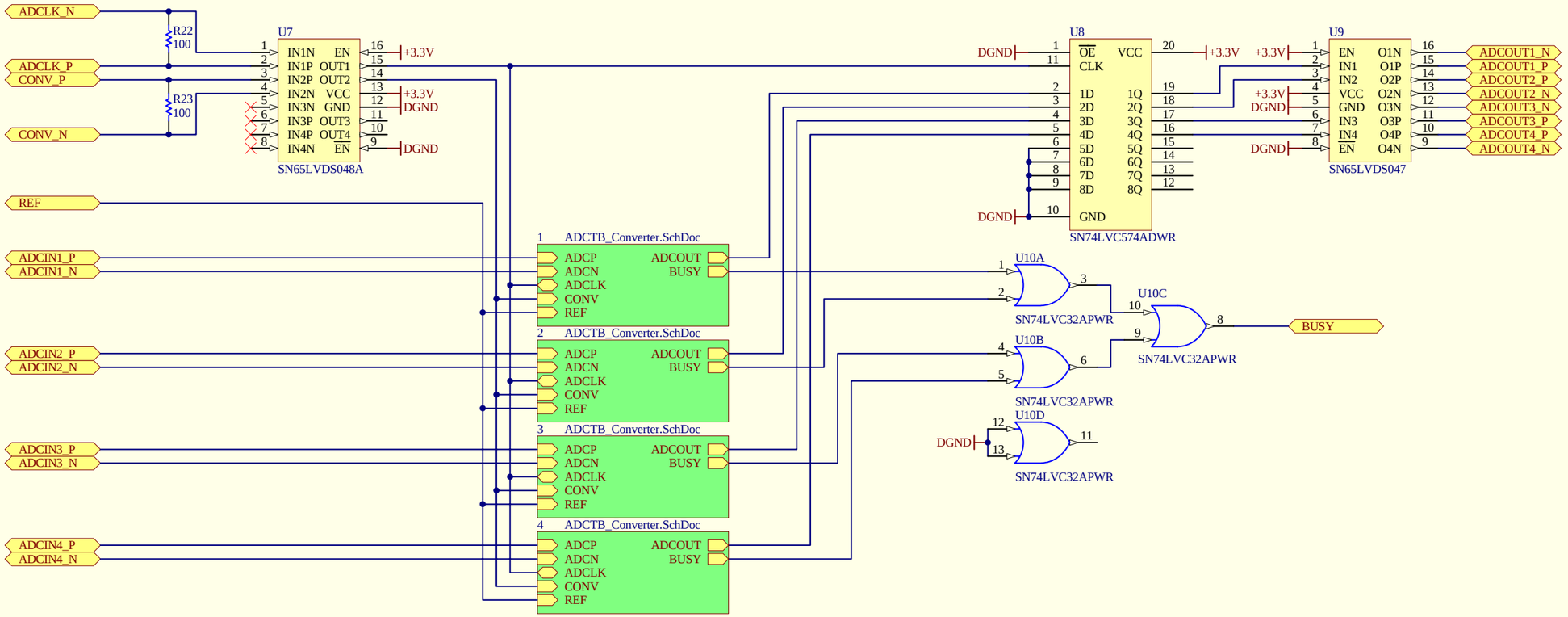
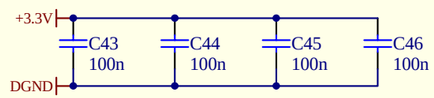


Rev.	Description	Date
A	Initial Release	June 2007
B	Corrected ADC drive voltages, cleaned up PCB layout.	August 2007
B1	As built of Rev. B. Tied U6 pin 25 to 3.3V, changed C2 & C12 to 820pF, tied U20 pin 7 to +AV1.	December 2007

Title: **ADC Test Board**	*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology*			LIGO
Size: B	DCC Number: D060535	SCH / PCB Revision: B1	Engineer: *Joshua R. Myers*	Date: 12/17/2007 Time: 12:49:46 PM
File: C:\Documents and Settings\jmyers\My Documents\LHOBoards\Joshua\ADC Test Board\Rev. B - As Built\ADCTB_Overview1.SchDoc				Sheet 1 of 5



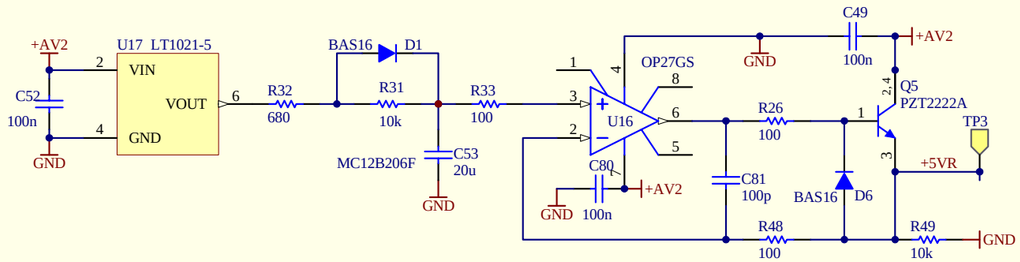


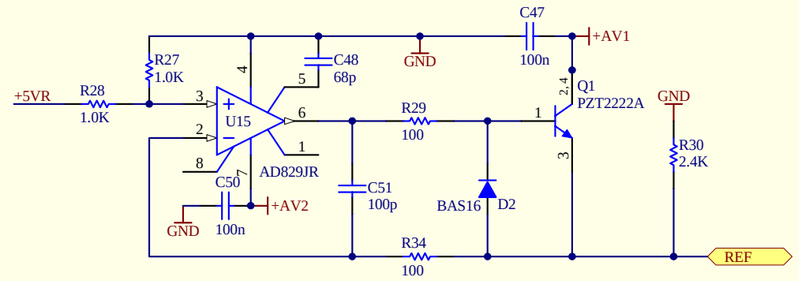
Title: *ADC Test Board: Quad ADC*			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology*	LIGO
Size: B	DCC Number: D060535	SCH / PCB Revision: B1	Engineer: *Joshua R. Myers*	Date: 12/17/2007 Time: 12:49:47 PM
File: C:\Documents and Settings\jmyers\My Documents\LHOBoards\Joshua\ADC Test Board\Rev. B - As Built\ADCTB_Quad.SchDoc				Sheet 2 of 5

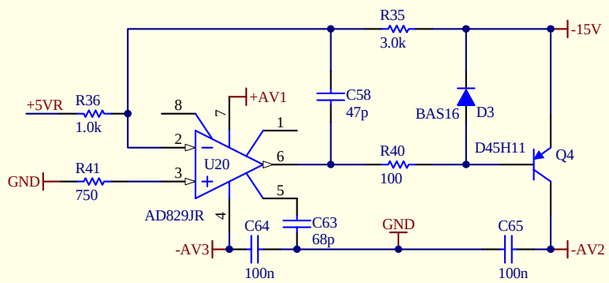
5th order Cheby, 200kHz cut-off, 0.5dB ripple

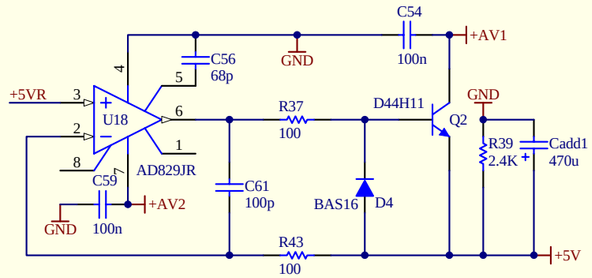
ADCN
ADCP
GND
+15V
-15V
AD829JR
U1
U2
U3
U4
U5
R1 100
R2 1k 0.05%
R3 1M
R4 1k 0.05%
R5 1k 0.05%
R6 100
R7 100
R8 10
R9 1k 0.05%
R10 1k 0.05%
R11 1M
R12 1k 0.05%
R13 100
R14 15
R15 2k 0.05%
R16 2k 0.05%
R17 680 0.05%
R18 750 0.05%
R19 15
R20 0
R21 100
C1 1u
C2 820p 1%
C3 1u
C4 68p
C5 1u
C6 2.2n 1%
C7 8.2n 5%
C8 1u
C9 68p
C10 1u
C11 68p
C12 820p 1%
C19 1u
C26 2.7n
C27 10n 1%
C28 1u
C29 1u
C30 68p
C34 120p 1%
C36 2.7n
C37 68p
C38 1u
C39 1u
TP1
TP2
+5V
+3.3V
DGND
C13 10u
C14 1u
C15 100n
C16 100n
C17 1u
C18 10u
C20 10u
C21 1u
C22 100n
C23 100n
C24 1u
C25 10u
C31 47u
C32 1u
C33 1u
C35 47u
C40 10u
C41 1u
C42 100n
REF
U6
AD7634
VCC
AVDD
DVDD
OVDD
VEE
AGND
RESET
PD
CNVST
BUSY
CS
RD
MODE0
MODE1
WARP
IMPULSE
TEN
BIPOL
IN+
IN-
REF
REFGND
REFBUFIN
PDREF
PDBUF
D0/OB/2C
D1/A0
D2/A1
D3
D4/DIVSCLK0
D5/DIVSCKL1
D6/EXT/INT
D7/INVSYNC
D8/INVSCKL
D9/RDC/SDIN
D10/SDOUT
D11/SCLK
D12/SYNC
D13/RDERROR
D14/HW/SW
D15/SPPDATA
D16/SPPCLK
D17/SPPEN
TEMP
CONV
BUSY
ADCOUT
ADCLK

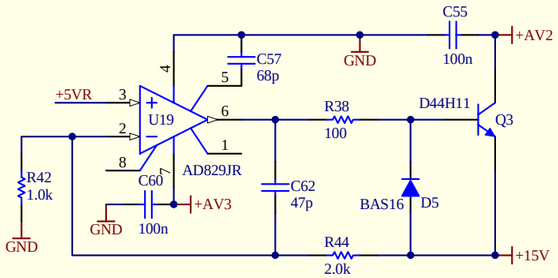
Title: ADC Test Board: Front End			LIGO Laboratory California Institute of Technology Massachusetts Institute of Technology	LIGO
Size: B	DCC Number: D060535	SCH / PCB Revision: B1	Engineer: Joshua R. Myers	Date: 12/17/2007 Time: 12:49:47 PM
File: C:\Documents and Settings\jmyers\My Documents\LHOBoards\Joshua\ADC Test Board\Rev. B - As Built\ADCTB_Conversion_Sch.SchDoc				Sheet 5 of 6

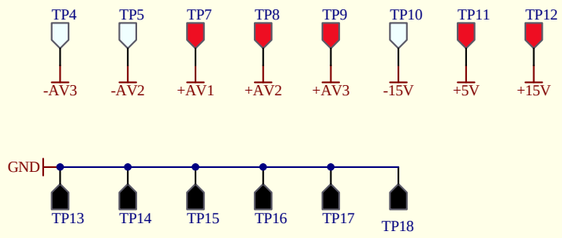


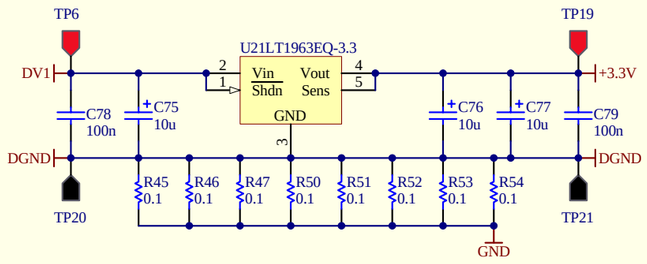




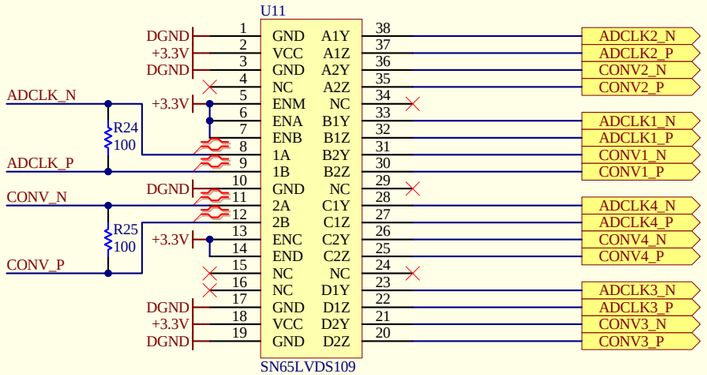


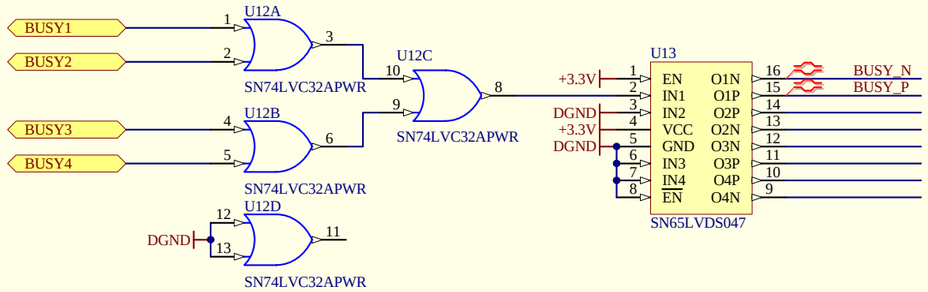


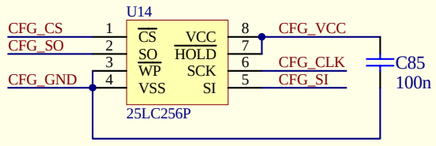


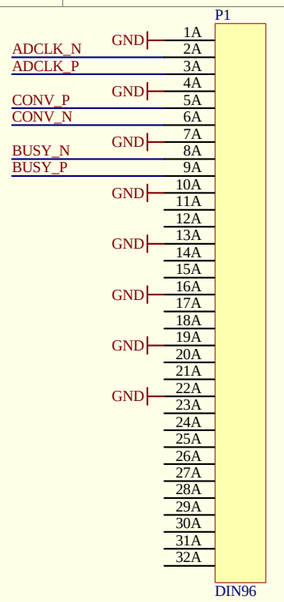


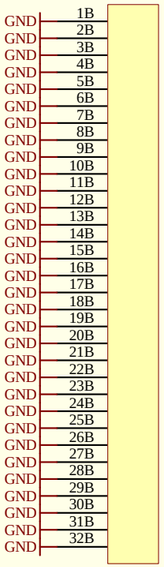
Title: **ADC Test Board: Power**			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology*	LIGO
Size: B	DCC Number: D060535	SCH / PCB Revision: B1	Engineer: *Joshua R. Myers*	Date: 12/17/2007 Time: 12:49:48 PM
File: C:\Documents and Settings\jmyers\My Documents\LHOBoards\Joshua\ADC Test Board\Rev. B - As Built\ADCTestBoardSheet4.SchDoc				Sheet 4 of 15

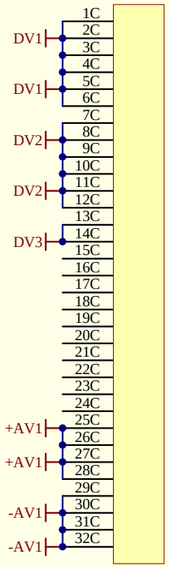


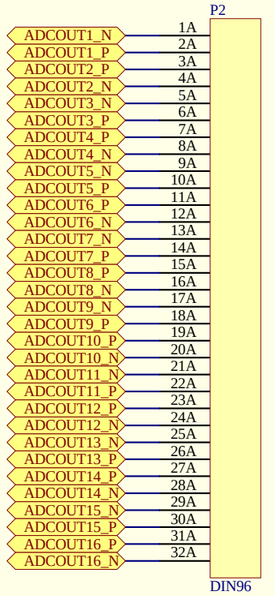


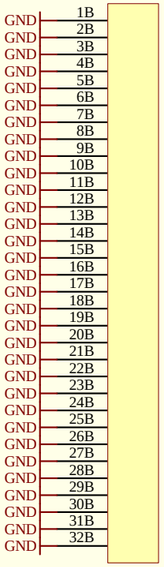


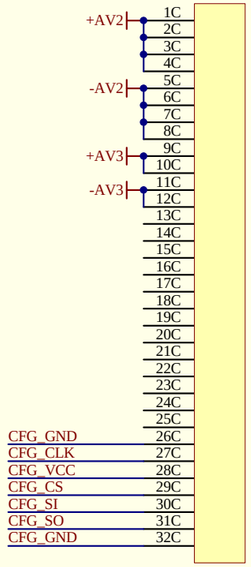


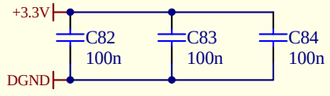












Title: **ADC Test Board: Interface**			*LIGO Laboratory* *California Institute of Technology* *Massachusetts Institute of Technology*
Size: B	DCC Number: D060535	SCH / PCB Revision: B1	Engineer: *Joshua R. Myers*
File: C:\Documents and Settings\jmyers\My Documents\LHOBoards\Joshua\ADC Test Board\Rev. B - As Built\ADCTestBoardInterface.SchDoc			Date: 12/17/2007 Time: 12:49:48 PM Sheet 5 of 5