

2X3 (LVEA 2k)

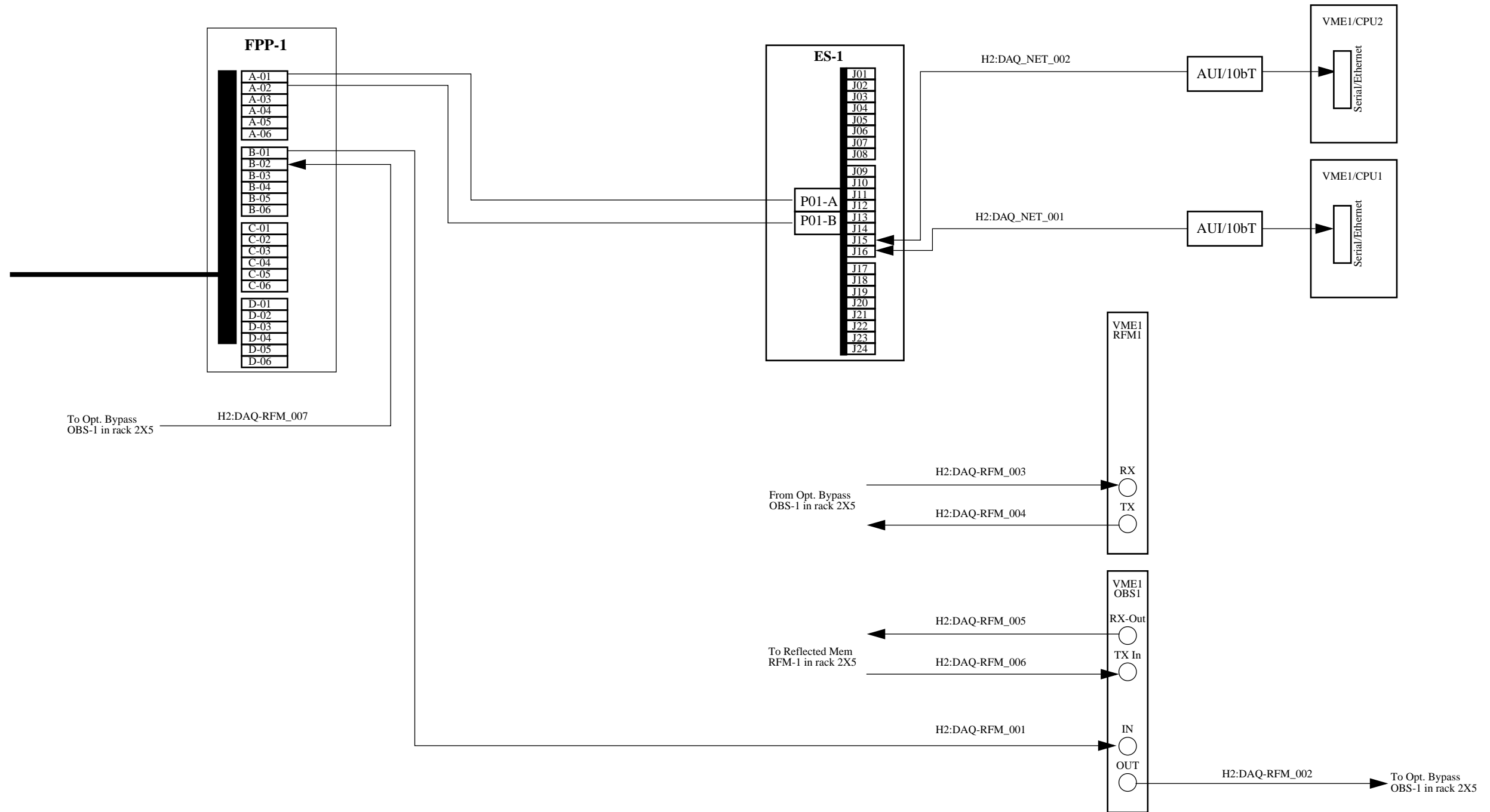
Rack Mount Components w/Locations

Loc	Description	Vendor	Model	Designator
01	Multi-Mode Fiber Optic Patch Panel			FPP-1
06	Ethernet Switch w/ATM Uplink	Fore	ES-3810	ES-1
07	Cable routing panduit	Panduit		CRP-1
09	IRIG-B Timing Fanout Chassis	Brandywine		IRIG-1
12	AVA-300 Video/ATM convertor	Fore	AVA-300	VIDEO-1
14	VME Crate			VME-1
23	DAQS Interconnect Chassis	LIGO		DAQSIC-1
24	DAQS Interconnect Chassis	LIGO		DAQSIC-2
26	DAQS Interconnect Chassis	LIGO		DAQSIC-3
27	DAQS Interconnect Chassis	LIGO		DAQSIC-4
29	DAQS Interconnect Chassis	LIGO		DAQSIC-5

VME Modules / Slot Assignments

Slot	Description	Vendor	Model	Designator
1	MIPS Processor	Heurikon	4700	uP-1
2	MIPS Processor	Heurikon	4700	uP-2
3	Reflected Memory	VMIC	5588DMA	RM-1
4	Optical Bypass Switch	VMIC		OBS-1
5	GPS Time Master	Brandywine	JK2	GPS-1
6	GPS Clock Master	Brandywine		GPS-2
7	Timing Master Fanout	LIGO		TMF-1
8	Timing Slave	LIGO		TS-1
9	ADC	ICS	110B1	ADC-1
10	ADC	ICS	110B1	ADC-2
11	ADC	ICS	110B1	ADC-3
12	ADC	ICS	110B1	ADC-4
13	ADC	ICS	110B1	ADC-5
14				
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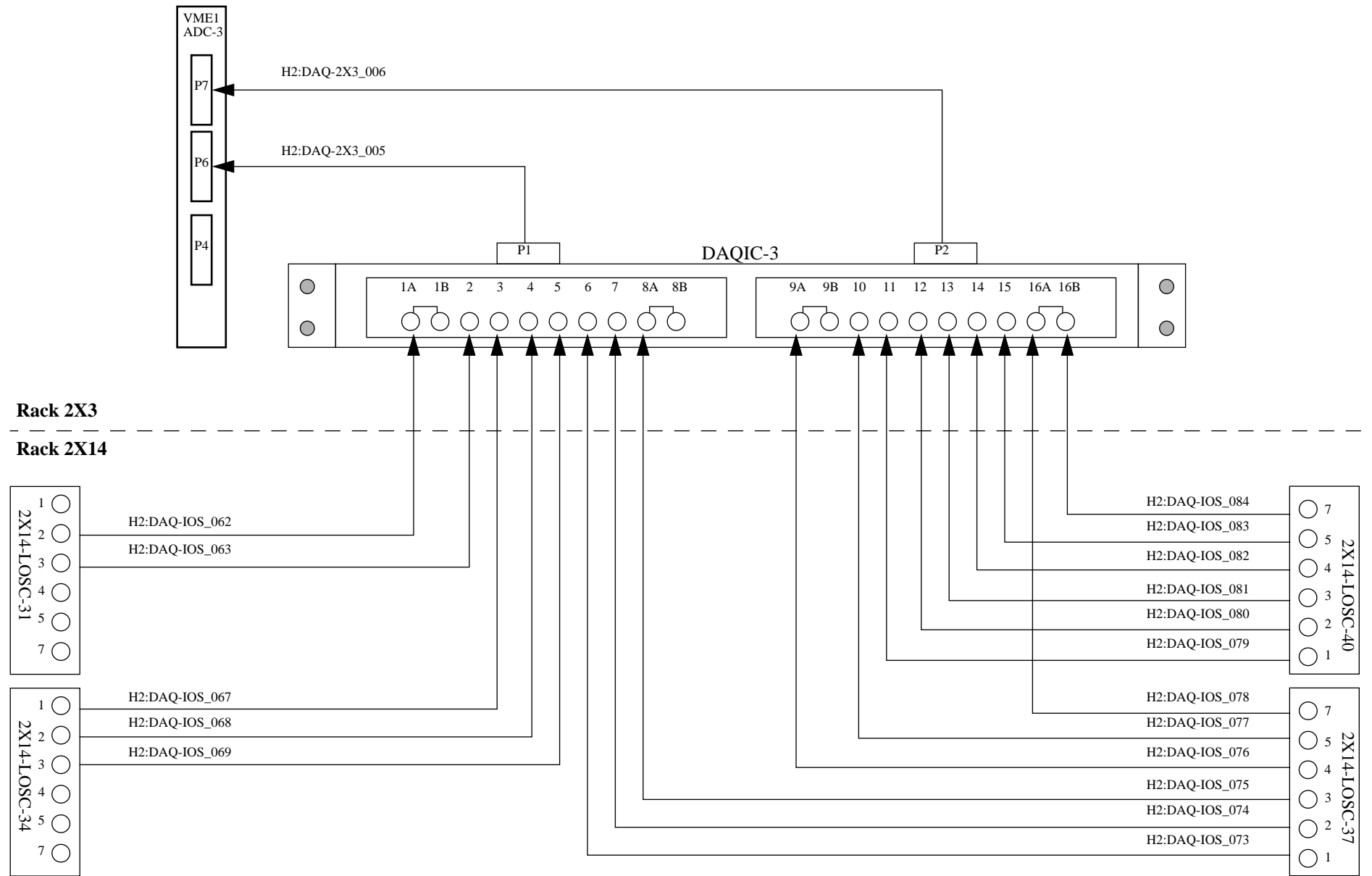
				UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR RACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS IN OUT, REMOVE ALL BURRS		File: /opt/CDS/c/docs/daq/drawings/dev/Rack_2X3.fm5 Last Modified Date: December 13, 1999		CURRENT REVISION APPROVAL				LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY			
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				USED ON:		DESCRIPTION		CHECKED		D.Barker		LHO		03 Oct 99	
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6				5		4		3		2		1		D990015-00-C	
REFERENCE DRAWINGS						ISSUE DESCRIPTION		SCALE		SHEET 1 of 8		STD		VER. 01	



				UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR RACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ± FINISHED SURFACE RMS BREAK CORNERS IN OUT, REMOVE ALL BURRS	File: /opt/CDS/c/docs/daq/drawings/dev/Rack_2X3.fm5 Last Modified Date: December 13, 1999				CURRENT REVISION APPROVAL				LIGO CALIFORNIA INSTITUTE OF TECHNOLOGY MASSACHUSETTS INSTITUTE OF TECHNOLOGY										
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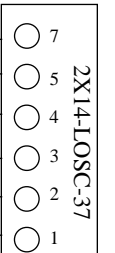
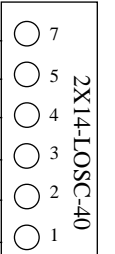
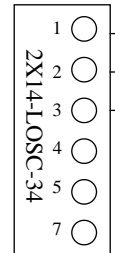
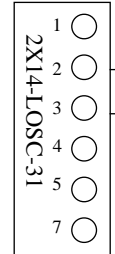
ADC3

Chan	Name	Rate
00	H2:-SUS-ITMX_COIL_UR	2048
01	H2:-SUS-ITMX_COIL_LR	2048
02	H2:-SUS-ITMX_COIL_SIDE	2048
03	H2:-SUS-ITMX_COIL_SUM	16384
04	H2:-SUS-ITMY_COIL_UL	2048
05	H2:-SUS-ITMY_COIL_LL	2048
06	H2:-SUS-ITMY_COIL_UR	2048
07	H2:-SUS-ITMY_COIL_LR	2048
08	H2:-SUS-ITMY_COIL_SIDE	2048
09	H2:-SUS-ITMY_COIL_SUM	16384
10	H2:-SUS-RCM_COIL_UL	2048
11	H2:-SUS-RCM_COIL_LL	2048
12	H2:-SUS-RCM_COIL_UR	2048
13	H2:-SUS-RCM_COIL_LR	2048
14	H2:-SUS-RCM_COIL_SIDE	2048
15	H2:-SUS-RCM_COIL_SUM	16384
16	H2:-SUS-RCM_SENSOR_UL	256
17	H2:-SUS-RCM_SENSOR_LL	256
18	H2:-SUS-RCM_SENSOR_UR	256
19	H2:-SUS-RCM_SENSOR_LR	256
20	H2:-SUS-BSM_COIL_UL	2048
21	H2:-SUS-BSM_COIL_LL	2048
22	H2:-SUS-BSM_COIL_UR	2048
23	H2:-SUS-BSM_COIL_LR	2048
24	H2:-SUS-BSM_COIL_SIDE	2048
25	H2:-SUS-BSM_COIL_SUM	16384
26	H2:-SUS-BSM_SENSOR_UL	256
27	H2:-SUS-BSM_SENSOR_LL	256
28	H2:-SUS-BSM_SENSOR_UR	256
29	H2:-SUS-BSM_SENSOR_LR	256
30	H2:-SUS-RCM_SENSOR_SIDE	256
31	H2:-SUS-BSM_SENSOR_SIDE	256
TOTAL (BTYES/SEC)		209920



Rack 2X3

Rack 2X14



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL ±
ANGULAR ± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
FINISHED SURFACE RMS
BREAK CORNERS IN OUT,
REMOVE ALL BURRS

File: /opt/CDS/c/docs/daq/drawings/dev/Rack_2X3.fm5
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Hanford CDS Rack Layout - 2X3
DAQS Interconnect Chassis
(2X3_DAQIC-3)

DO NOT SCALE THIS DRAWING
USED ON:
NEXT ASS'Y:

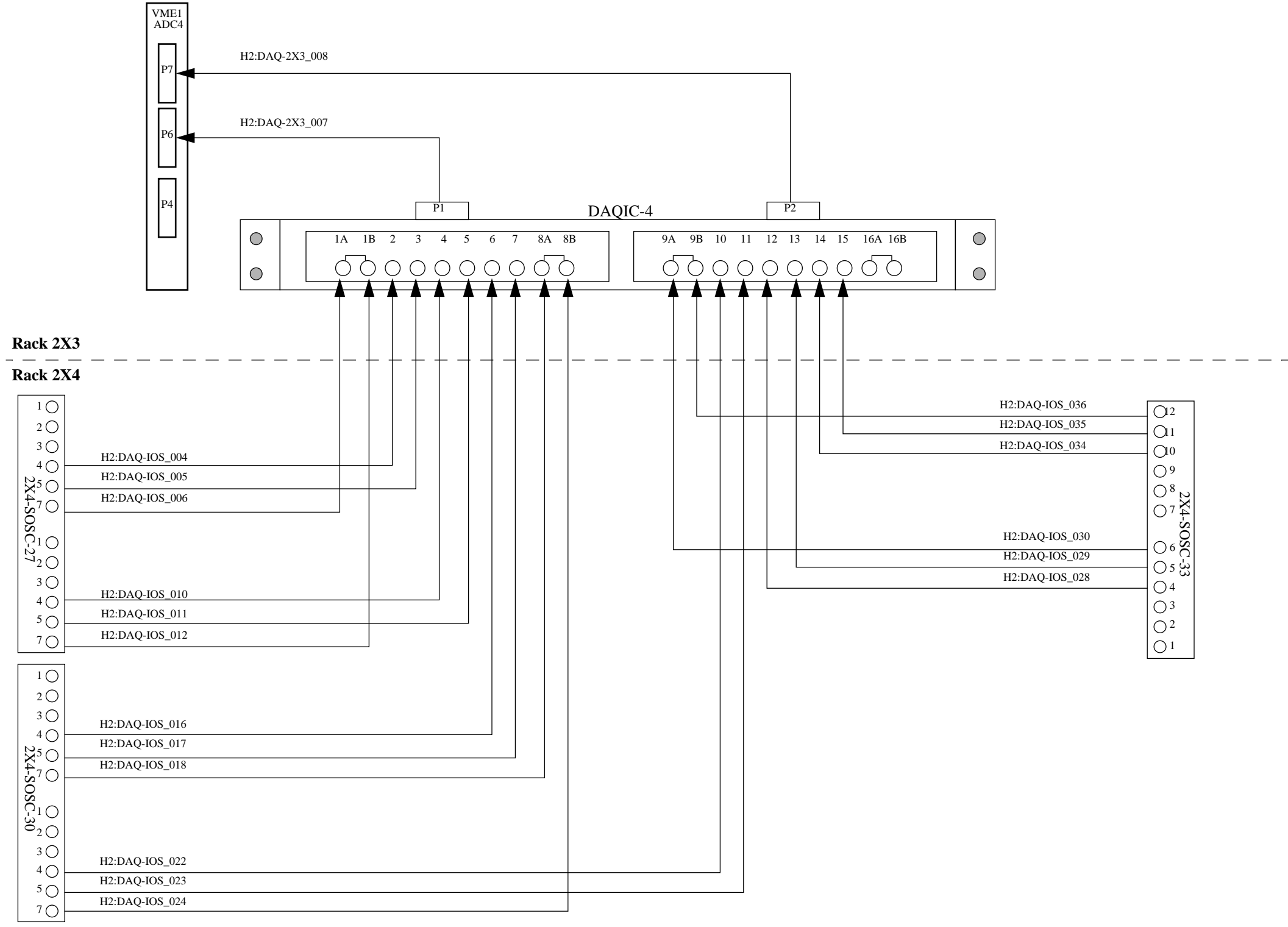
REV	DESCRIPTION	SHEETS EFFECTED	DATE
	ISSUE DESCRIPTION		

SIZE	DWG. NO.
B	D990015-00-C

SCALE	SHEET	STD	VER.
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ADC4

Chan	Name	Rate
00	H2:SUS-MC1_SENSOR_SIDE	256
01	H2:SUS-MC2_SENSOR_SIDE	256
02	H2:SUS-MC1_SENSOR_UL	256
03	H2:SUS-MC1_SENSOR_LL	256
04	H2:SUS-MC1_SENSOR_UR	256
05	H2:SUS-MC1_SENSOR_LR	256
06	H2:SUS-MC2_SENSOR_UL	256
07	H2:SUS-MC2_SENSOR_LL	256
08	H2:SUS-MC2_SENSOR_UR	256
09	H2:SUS-MC2_SENSOR_LR	256
10	H2:SUS-MC3_SENSOR_UL	256
11	H2:SUS-MC3_SENSOR_LL	256
12	H2:SUS-MC3_SENSOR_UR	256
13	H2:SUS-MC3_SENSOR_LR	256
14	H2:SUS-MC3_SENSOR_SIDE	256
15	H2:SUS-SM1_SENSOR_SIDE	256
16	H2:SUS-SM2_SENSOR_SIDE	256
17	H2:SUS-MMT1_SENSOR_SIDE	256
18	H2:SUS-SM1_SENSOR_UL	256
19	H2:SUS-SM1_SENSOR_LL	256
20	H2:SUS-SM1_SENSOR_UR	256
21	H2:SUS-SM1_SENSOR_LR	256
22	H2:SUS-SM2_SENSOR_UL	256
23	H2:SUS-SM2_SENSOR_LL	256
24	H2:SUS-SM2_SENSOR_UR	256
25	H2:SUS-SM2_SENSOR_LR	256
26	H2:SUS-MMT1_SENSOR_UL	256
27	H2:SUS-MMT1_SENSOR_LL	256
28	H2:SUS-MMT1_SENSOR_UR	256
29	H2:SUS-MMT1_SENSOR_LR	256
30		
31		
TOTAL (BTYES/SEC)		15360



UNLESS OTHERWISE SPECIFIED
 DIMENSIONS ARE IN INCHES
 TOLERANCES:
 FRACTIONAL ±
 ANGULAR MACH ± BEND ±
 TWO PLACE DECIMAL ±
 THREE PLACE DECIMAL ±
 FINISHED SURFACE RMS
 BREAK CORNERS IN OUT,
 REMOVE ALL BURRS

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**Hanford CDS Rack Layout - 2X3
 DAQS Interconnect Chassis
 (2X3_DAQIC-4)**

DWG. NO.	DESCRIPTION	DWG. NO.	DESCRIPTION	USED ON:	REV	DESCRIPTION	SHEETS EFFECTED	DATE	SCALE	DWG. NO.	REV.
6	REFERENCE DRAWINGS	5		NEXT ASS'Y:		ISSUE DESCRIPTION			1:1	D990015-00-C	
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