LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY

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High Bandwidth FSS Card

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1 Design Consideration

The aim of the design was to increase the bandwidth of the Frequency Stabilization Servo (FSS) to at least 1 MHz. The design employs an electronic "bypass" topology[1] pioneered by J. L. Hall and others in the early 1980's. This technique, originally invented to deal with bubbles in dye laser media, routes the high frequency signals around the high voltage, bandwidth limited components required to compensate large audio-frequency wavelength excursions. The design works because the efficacy of the phase correcting Pockels cell increases with frequency, while RMS frequency errors of the laser decrease with frequency above a few tens of kHz. High voltage corrections are thus only required at intermediate frequencies (~10 kHz). Despite the fact that the bandwidth-determining high frequency part of the servo does not require high voltage, careful regard needs to be paid to the slew rate, as excessive noise at higher frequencies can saturate the amplifiers around 200 kHz.

For the present tests a design was built around an existing FSS card based on another architecture, so some compromises were endured to make best use of parts and traces that already existed. A board designed and built from scratch on these principles will likely perform (and definitely look) better.

2 Schematics

The FSS has four main paths described in the following table:

Path Name	Freq. Range	Actuator	Frequency Response
Slow Path	< 1 Hz	NPRO Crystal Temp	
Fast Path	DC-40 kHz	NPRO PZT	Flat
High Voltage PC Path	40 kHz-330 kHz	Phase correcting PC	Phase
High Frequency PC Path	>330 kHz	Phase correcting PC	Phase

Hand drawn schematics are shown as Figure 2-1, 2-2 and 2-3

3 Performance

The performance of the card is illustrated in Figure 3-1. Figure 3-1 shows the transfer function from the PC/fast path electronic split to the PC voltage output. This plot shows the smooth cross over between the High Voltage PC Path and the High Frequency PC path at 330 kHz. It also shows that the unwanted phase lag at 1 MHz is only 8 degrees. With this stage and the Savage/Swinberg idea of mounting the FSS card next to the laser on the PSL table a FSS bandwidth in excess of 3 MHz should be achievable.

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[1] J. L. Hall and T. W. Hansch, *Opt. Lett.* **9** (11), p. 502 (1984); R.W.P. Drever, J.L. Hall, F.V. Kowalski, J. Hough, G.M. Ford, A.J. Munley, and H. Ward, *Appl. Phys. B* **31**, p. 97 (1983); G.A. Kerr, N.A. Robertson, J. Hough and C.N. Man, *Appl. Phys. B* **37**, p. 11 (1985); M. Zucker, Ph.D. dissertation, California Institute of Technology, p. 80 (1988).

Figure 3-2 show the full electronic transfer function, from Test In 1 to the voltage on the pockel cell. The additional 27 degrees of phase lag was trace to an AD 747 Op Amp in the common path (Op Amp U1), this was almost completely fixed when this Op Amp was exchanged for an AD847. The slew rate of OP Amp U11 needs to be reasonably high to prevent saturation from excessive frequency noise around 200 kHz

The open loop transfer function from this board is shown as Figure 3-3. There is an uncompensated pole from the RFPD in this circuit. This accounts for at least 50 degrees of phase loss at 1 MHz . A phase margin of at least 45 degrees can be obtained with a unity gain frequency of 900 kHz. At least another 10 degrees is lost due to optical and electrical propagation delays.

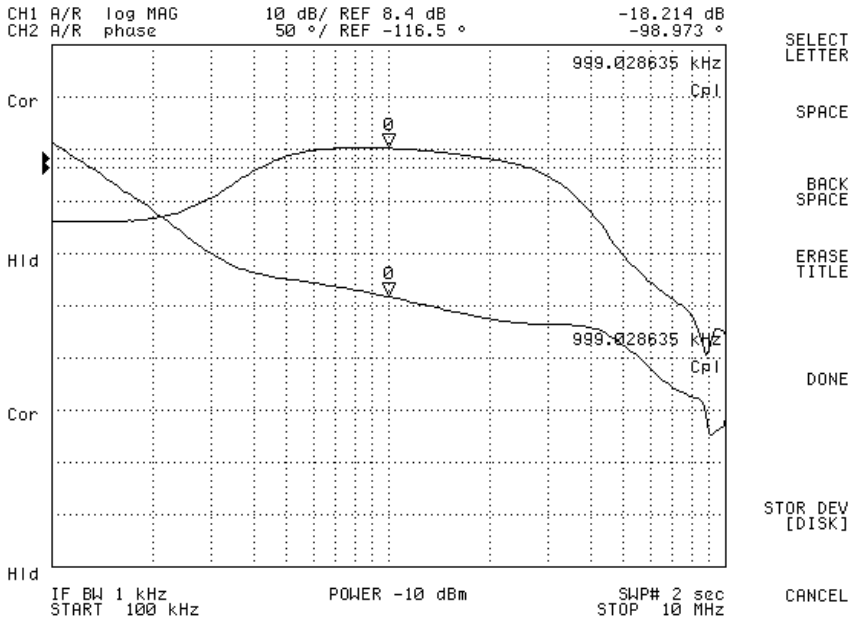


Figure 3-1 Transfer function from the PC Path split to the PC

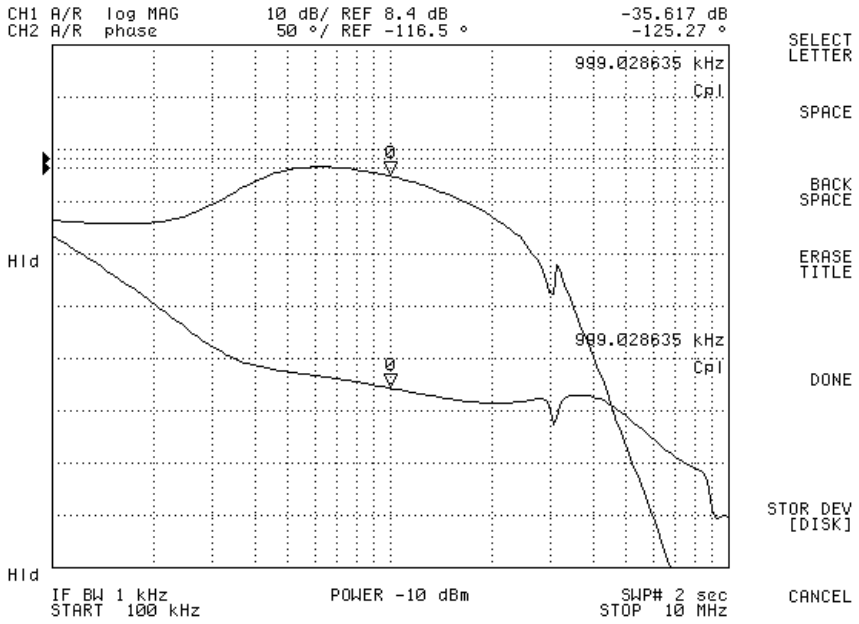


Figure 3-2 Transfer function from Test 1 In to voltage on PC

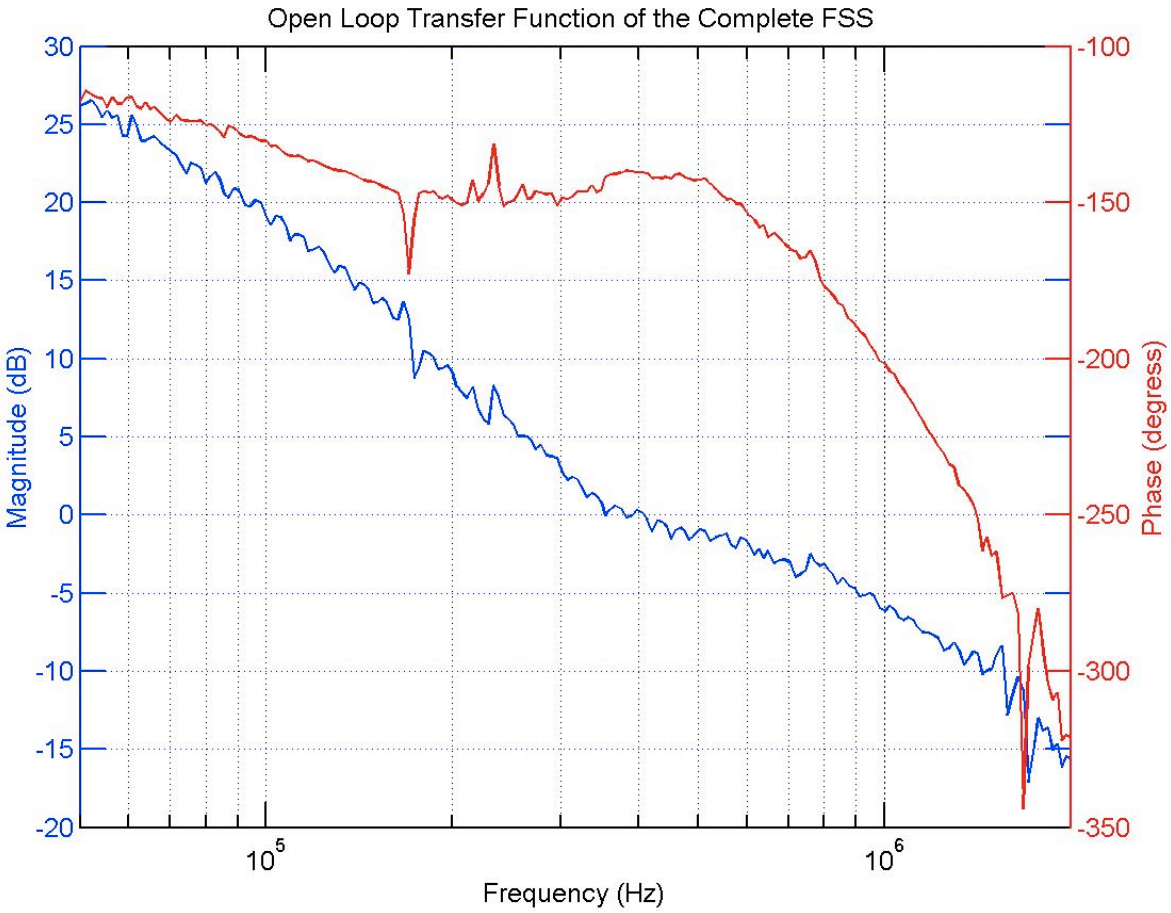
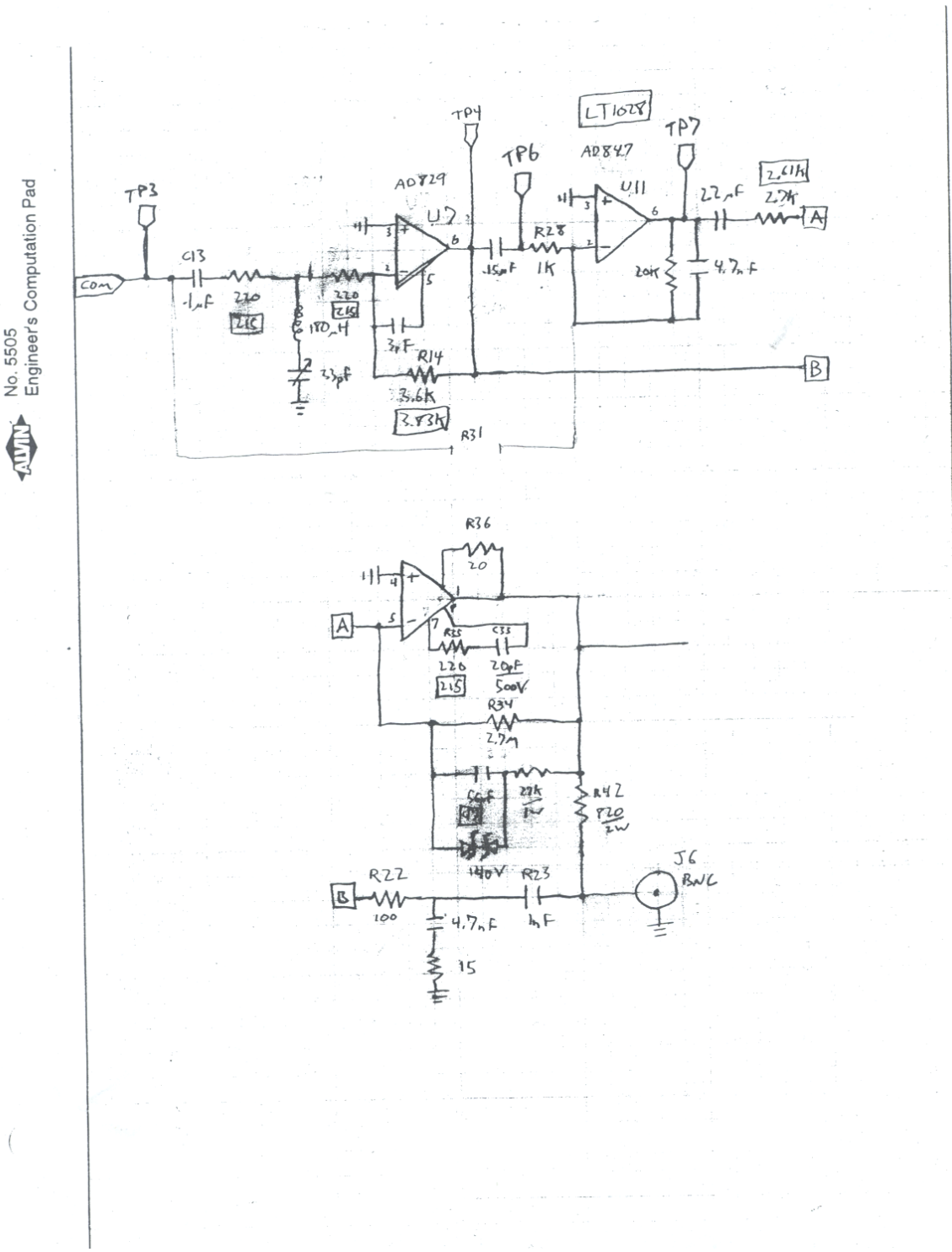
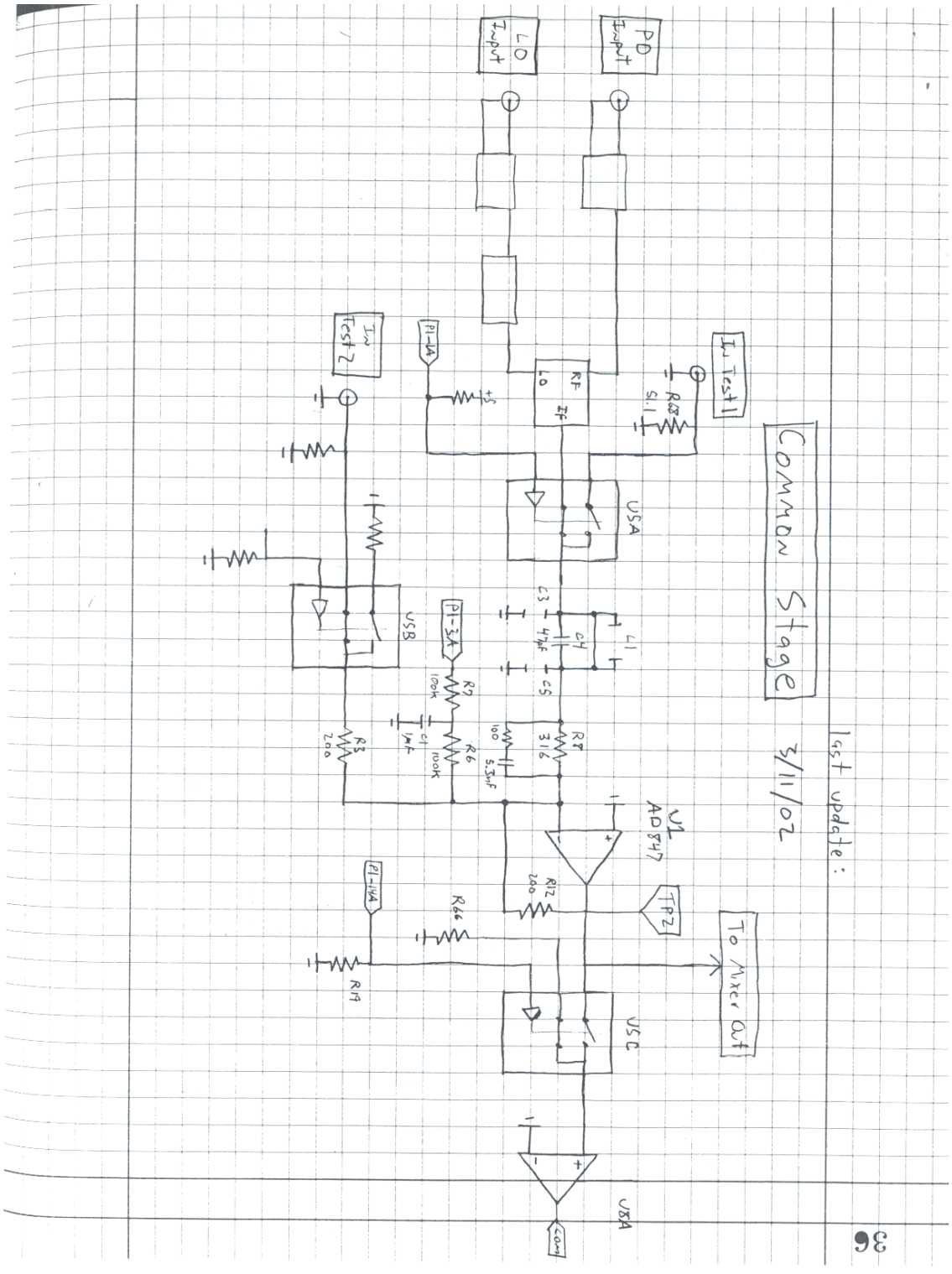


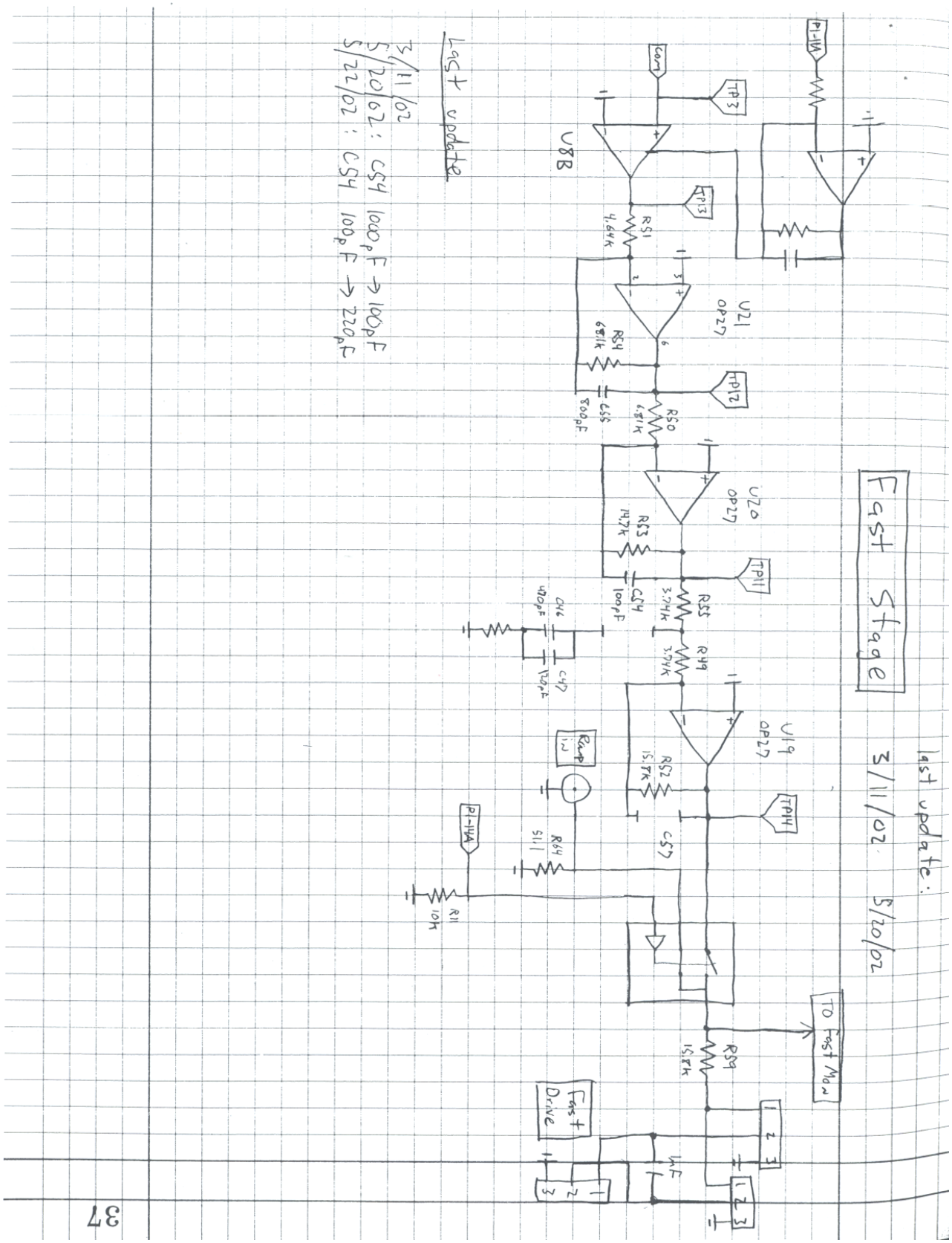
Figure 3-3 FSS Open loop transfer function

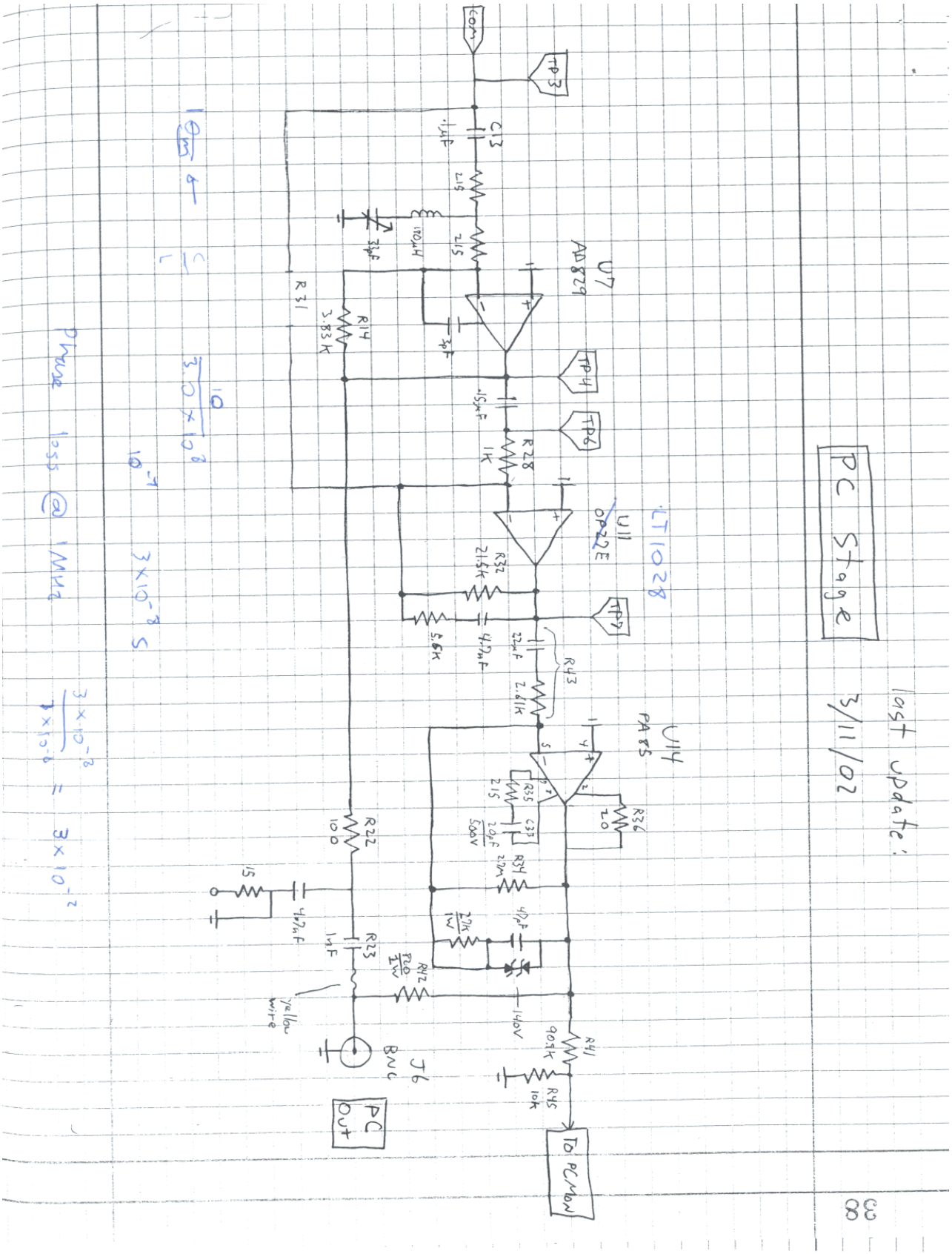
Appendix 1 High Frequency Bypass Design



Appendix 2 Complete Schematic of Servo Card




Fast Stage
last update: 3/11/02 5/20/02
Last update
3/11/02
5/20/02: C54 1000pF → 100pF
5/22/02: C54 100pF → 220pF
U8B
U21 OP27
U20 OP27
U19 OP27
TP3
TP13
TP12
TP11
TP14
R51 4.64K
R54 681K
R50 681K
R53 147K
R55 3.74K
R49 3.74K
R52 15.8K
R59 15.8K
R64 511
R11 10K
C54 100pF
C56 470pF
C47 150pF
C57
C58 800pF
Ramp 1Hz
P1-14A
TO Fast Mon
Fast Drive
1mF



$\frac{10}{3.0\times10^{8}} = 3\times10^{-8}$

10^{-7} 3×10^{-8} s

Phase loss @ 1MHz $\frac{3\times10^{-8}}{1\times10^{-6}} = 3\times10^{-2}$