

LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
-LIGO-
CALIFORNIA INSTITUTE OF TECHNOLOGY
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Design Document	LIGO-T030078-00- C	04/17/03
LIGO Digital Suspension Control Watchdog System		
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This is an internal working note
of the LIGO Project.

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Overview

This document describes the design and implementation of LIGO Digital Suspension Control Watchdog System as per requirements identified in the LIGO document T030015-00-C. The document also describes the implementation schedule, including the hardware and software tasks and establishes the guidelines and procedures for changes made to the existing system. A brief overview of the control system is provided next to indicate the signal interconnections of different modules that make up the control system.

The Digital Suspension Control System

The Digital Suspension Control of LIGO is the primary sensing mechanism of the interferometer comprising the electronic controls of the physical suspension mirrors that form the LIGO Large Optic Systems (LOS) and the Small Optic Systems (SOS). Each mirror of the DSC System is provided with a dedicated VME front-end controller, where the decision is being made of how much current should be placed on the individual mirror coils. A Control Signal in the form of a control current is being generated at the Front-End and travels through different path before reaching the final stage of Coil Driver board, where it is being amplified and injected into the mirror coils for positioning of the mirrors. There is also a supplemental Bias Current to the Coil Driver board that further stabilizes the motion of the mirrors as required for finer control.

The following is a description of how the Control and Biasing signals are being distributed.

Control Signals

The Front-End uses Pentek 6102 D/A converter for generating the Control Signals for all optics, but the output for the large optics including BS, RM, ITMX, ITMY, ETMX and ETMY is being produced at the rate of 16KHz, whereas for the small optics including MC1, MC2, MC3, SM1, MMT1, MMT2 and MMT3 the rate is 2KHz.

The block diagram in Figure 1.1 depicts the Control Signal path for the large optics systems including BS, RM, ITMX, ITMY, ETMX and ETMY.

The block diagram in Figure 1.2 depicts the Control Signal path for the small optics system of MC1, MC2, MC3, SM1, MMT1, MMT2 and MMT3.

Large Optics System Control

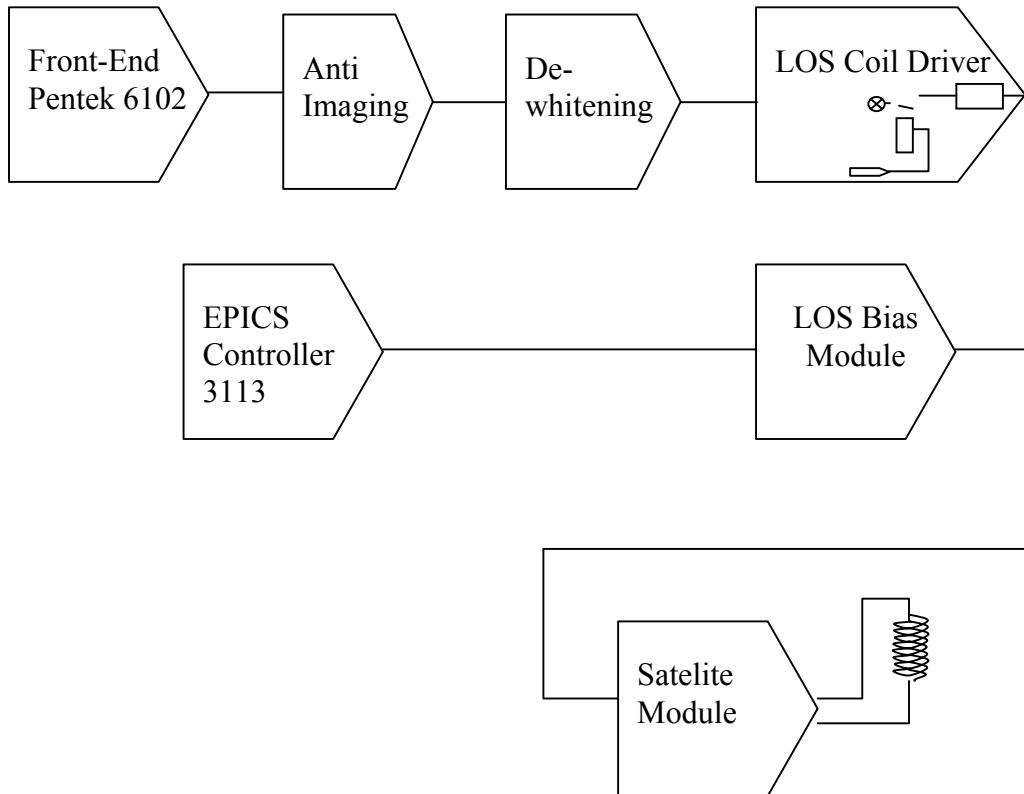


Figure 1.1. The Large Optics Control Signals (BS, RM, ITMX, ITMY, ETMX and ETMY) from the Pentek 6102 D/A Analog Output boards pass through the Anti-Imaging (D000186) board followed by the Universal Dewhiting (D000183) board before being fed into the LOS Coil Driver (D000325) board for amplification and injection.

Small Optics System Control

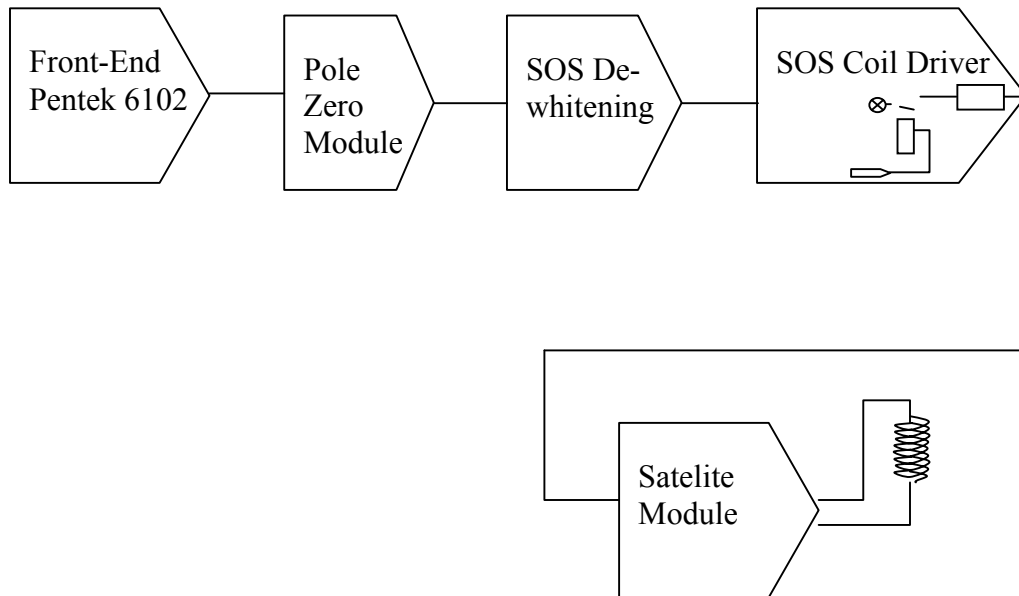


Figure 1.2. The Small Optics Control Signals (MC1, MC2, MC3, SM1, MMT1, MMT2 and MMT3) from the Pentek 6102 D/A Analog Output pass through the SOS Pole/Zero Module (D010284) and the SOS Dewhitening board (D000316) before being fed into the SOS Coil Driver board (D010001) for amplification and injection.

Biasing Current

Besides the Control Current there is an auxiliary Biasing Current being injected as a supplemental current to further stabilize the mirror motion, but it is available to large optics systems only. The LOS Bias Module (D000341) receives a Bias Current Signal as an input and drives an amplifier that produces a proportional high current, similar to the Control Signal of the LOS Coil Driver board. The amplified current from the Bias module and the amplified current from the Control Signals are summed together and injected into the mirror coil as the final step. The summation is being done in the LOS Coil Driver board as shown in the block diagram of Figure 1.1.

Note: the Bias Current is provided to the Large Optics System only.

Monitoring the Coil Current

It is important that the coils of the optics systems are protected from an inadvertent overdrive of the input current, as the environment is prohibitive of failures. Any damage to the coil means a total shutdown of the system for weeks. A fault protection scheme is currently being implemented to protect the system from such a catastrophic failure and also, care has been given to the design of the hardware that monitoring points are available for an effective implementation of a protection scheme using software algorithms. The figure 1.3 displays the available monitoring points on a typical large optics system and the figure 1.4 displays the small optics systems monitoring points.

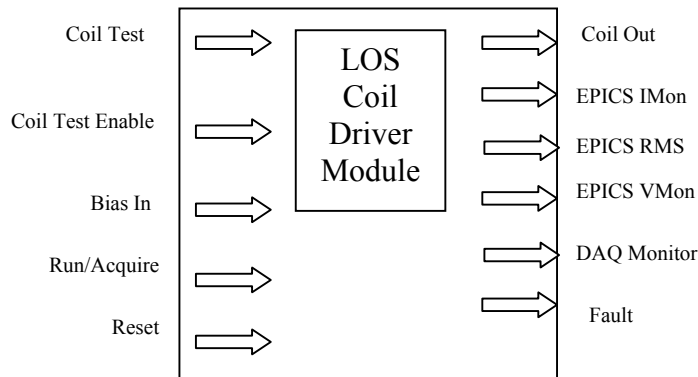


Figure 1.3 The Control and monitoring signals of a generic Coil in the LOS Coil Driver Module

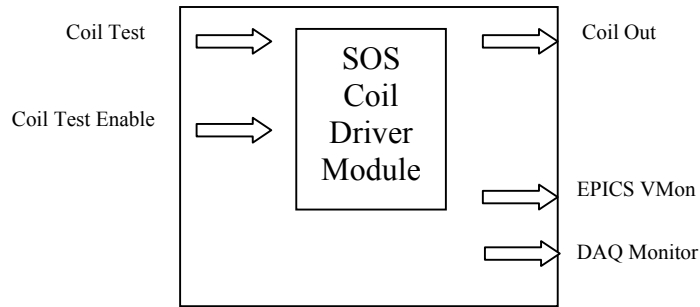


Figure 1.4 The Control and monitoring signals of a generic Coil in the LOS Coil Driver Module

The following section describes the existing fault protection scheme implemented for the DSC system.

Fault Protection

Although the burden of protecting the coil from the excess current is mainly a hardware design responsibility, such as placing fuses, implanting watchdog relays and putting current limiting resistors along the current path, but it is no solace that a blown fuse has protected the mighty OSEM or a burn-out resistor was found defending from culprit overdrive coil current. Software solution is more desirable as it is easy to implement and provides flexibility of detecting error conditions that are very hard to detect in otherwise hardware solutions, such as frequency dependent power output that exceeds required limit. Next, we will look at the existing software solution being implemented in the Digital Suspension Control System of LIGO and later discuss ways to improve the design.

Existing Software Solution

There is a SPST switch on the LOS Coil Driver module in the path of each coil Control Signal. The switch in-turn is controlled by a push-pull relay that is engaged by software signals from the XYCOM 220 digital output of the EPICS controller (11susaux10). The control of the XYCOM 220 is the primary mechanism of removing the Control Current signal from the LOS Coil Driver board. The following is the current software implementation of actuating the relays that enables or disables the SPST switch.

MEDM Operated Switches:

The MEDM screen of each optic system is provided with a simulated switch that effectively turns on and off the Control Signal to the LOS Coil Driver module.

Compare with a max Photo Diode output:

The mean value of the output current of each Photo Diode (PDMon) is being calculated for the duration of .2 second sampling. The output current is then compared with the mean to determine the oscillation the mirror is being subjected to. If the value exceeds a predefined user selectable max RMS value then the Control Signal to the Coil Driver is turned off and the MEDM screen shows a change in color from green to red. The operator is required to take appropriate action such as disable the “Acquire Mode” of the optics.

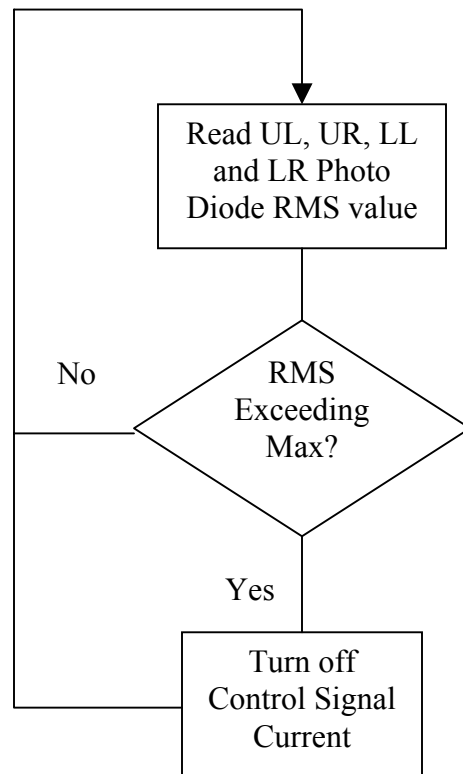


Figure 1.5. Algorithm for detecting oscillation of the mirror using Photo Diode current

Existing Hardware Solution

It has been determined that a sustained input of 200 ma current for one sec duration is detrimental to the coil. A slow-blow fuse is provided to protect the circuitry from this adverse condition.

There is also a built-in hardware integrator and comparator on the LOS Coil driver module that produces a fault condition upon detecting the overdrive current of 200 ma. But at present it is not being used for any purpose.

Frequent failures have shown that a more comprehensive watchdog system is required for the digital suspension control. A design and implementation scheme of such is being discussed next.

Implementing Digital Suspension Control Watchdog System

The design requirements as specified in the LIGO document T030015-00-C, identify the following preventive measures and when implemented could reduce the risk of potential failures,

- Provide user selectable Watchdog Trip set points
- Provide EPICS Alarm and warning levels set points
- Limit the user entries of Trip Levels to a safer limit.
- Bring the system to a known state at power-up time using EPICS backup and restore.
- Prevent Rail-to-Rail motion of the mirrors.
- Identify dead local sensors channels
- Identify dead Coil Channels.
- Prevent Excess Control Voltage and Current to the Coils
- Prevent the current supply to the coils in case of a Front-End failure

Watchdog System hardware enhancements

Each VME subsystem is to be augmented with a VMEbus Watchdog Board (LIGO Document T980050-00-C) providing a failsafe mechanism of disconnecting the control current in case of power loss to the front-end system. **It should be noted that the Watchdog board only provides protection to the control current going in to the Coil Driver board but not the current from the Coil Driver and the biasing current that is injected into the OSEM coils.**

LOS Wiring modifications

In the new scheme of relay control only one signal from the XYCom220 board (11susaux10) is being used to control all five relays of the Coil Driver board as shown in the Figure 1.6. The signal passes through the Watchdog relay switch before reaching the LOS Coil Driver relays. See LIGO Drawing D010035 for the actual pin numbers and connections to the cross-connect of the LOS rack mount.

Since each VME crate can accommodate only one Watchdog board providing four watchdog relays per system, while the LOS Coil Driver board provides independent control to all five relays (Upper Left, Lower Left, Upper Right, Lower Right and Side), there has to be a compromise of how much watchdog protection we can provide to the system. It has been decided that all five relays will be tied together so all of them could be controlled by a single watchdog relay. In the new system a comparable soft switch must be implemented that would act as SPST switch to the individual relays, as it is not feasible to have five independent watchdog relays in the hardware.

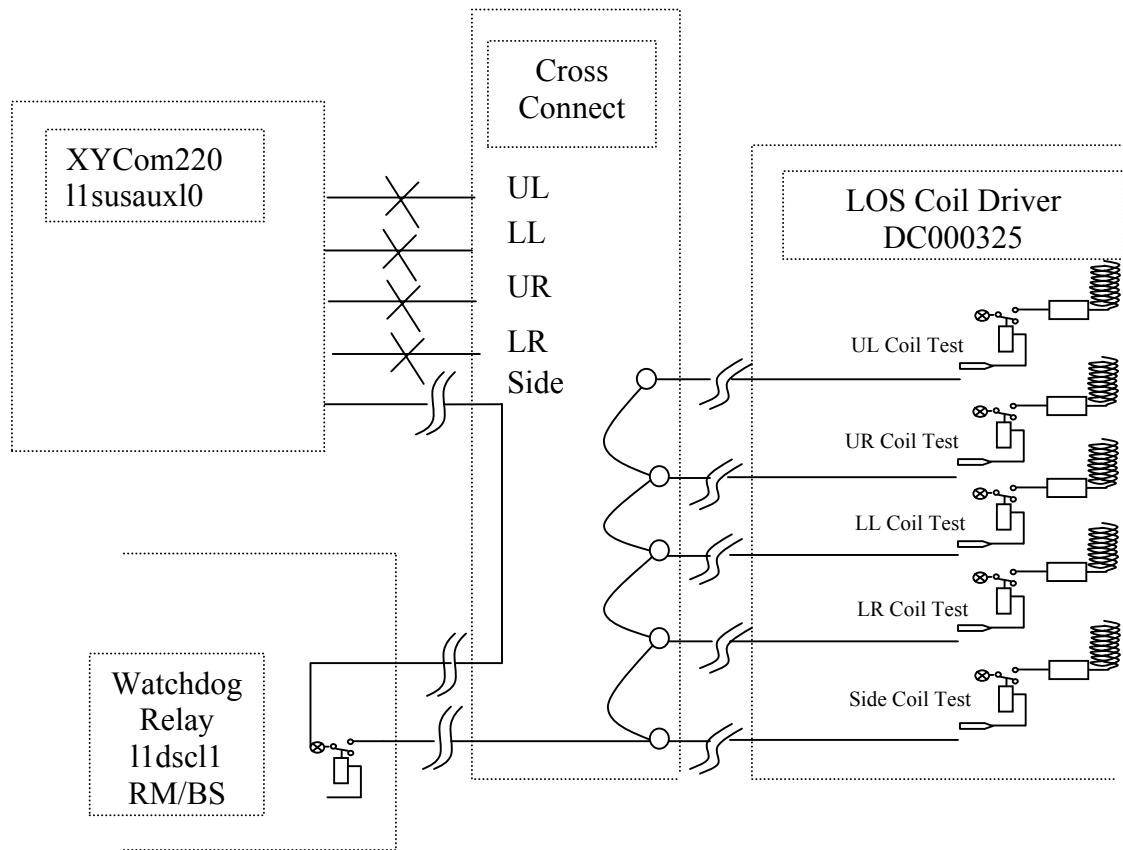


Figure 1.6. A generic scheme of adding a watchdog Relay to the Large Optics System

Watchdog System software enhancements

The followings are the software enhancement to the existing system,

RMS Coil Current Monitoring

The RMS value from the LOS Coil Driver board will be compared with a preset value and turn off the Control Signal and Bias Signal if the signal exceeds the max value.

Algorithm to Detect Rail to Rail motion

Software routines will be added to determine the rail-to-rail motion of the optics system similar to the scheme of oscillation detection of the Photo Diode current. The object files of 11susauxl0, 11iscauxex and 11iscauxey are to be modified to implement the algorithm.

The flowchart of Figure 1.7 describing the algorithm for detecting Rail-to-Rail motion.

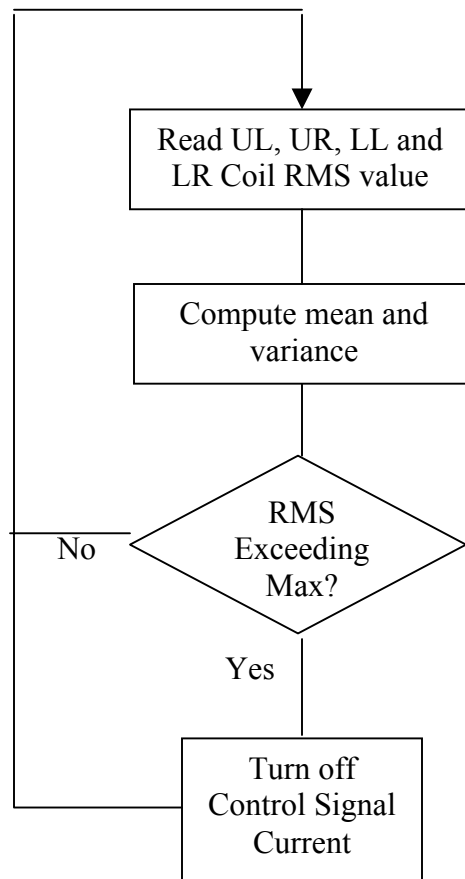


Figure 1.7. Algorithm for detecting Rail-to-Rail motion of the mirror using RMS value of the Coil Current

Watchdog timing board periodic access routine

/cvs/cds/generic/Pentium/watchdog.o

The routine is being executed in the VME front-end controller providing the periodic heartbeat to the Watchdog board. A failure in the front-end causes the Watchdog to trip, disengaging the current to the Coil Driver board.

The following address is assigned to the Watchdog board

```
#define WATCHDOG 0xfeffffffe;  
unsigned short * WD = (unsigned short *) WATCHDOG;
```

The following macro should be called during the system initialization.

```
#define WATCHDOG_INIT * WD = (unsigned short)0x8000;
```

The following macro should be called once every second during normal execution

```
#define WATCHDOG_TICK * WD =(unsigned short) 0x4000;
```

EPICS User interface for user selectable trip set points

/cvs/cds/medm/watchdogtrip.adl

The following EPICS channel provides the necessary user interface of setting the trip set points describing the maximum variance of the coil RMS value.

```
?1:SUS-????_COIL_MAX_VAR
```

Setup EPICS warning levels

The database records of l1susauxl0, l1iscauxex and l1iscauxey are modified for the new HIHI HILO Epics warning levels.

The following EPICS channels warning levels are set for 200ma limit as follows,
The conversion factor ASLO = 0.0004883 per ma count X 200 ma = 0.8

```
?1:SUS_????_??RMSMon HIHI 0.8  
?1:SUS_????_??RMSMon LOLO -0.8
```

BURT capability

The “saverequest” files of l1susauxl0, l1iscauxex and l1iscauxey Epics controllers are modified to take into considerations of the channels being added for the new Watchdog system.

Software routines to detect Dead coils and sensors

A dead Coil shorted to ground is hard to detect, while it is easy to verify that that a Coil is showing an open connection. Comparing VMon and IMon from the coil driver board provides enough information to decipher a problem with open Coil.

Task List

The following is the list of hardware and software tasks and the schedule of completion based on the requirements specified in the previous section,

Software Tasks

1. Watchdog timing board periodic access routine (20 Hrs)
2. EPICS User interface for user selectable trip set points (40 Hrs)
3. Setup EPICS warning levels (20 Hrs)
4. Add BURT capability (10 Hrs)
5. Develop algorithm to detect Rail to Rail motion (40 Hrs)
6. Develop software routines to detect dead Coils and sensors (30 Hrs)

Hardware Tasks

1. Procure and install Watchdog Timing Cards for six LOS (40 Hrs)
2. Modifications to the wirings of the LOS Coil relay input (40 Hrs)
3. Test and verify Software and Hardware integration (40 Hrs)

Watchdog System Components

The following VME based front-end subsystems control the different LOS suspension mechanisms providing the control current to the LOS Coil Driver board, that in-turn provides the high current actuating the OSEM coil magnets causing the physical mirror motions.

11dsc11	->	Recycling Mirror (RM) and Beam Splitter (BS)
11dsc12	->	In Test Mass X (ITMX) and In Test Mass Y (ITMY)
11iscex	->	End Test Mass X (ETMX)
11iscey	->	End Test Mass Y (ETMY)

The following VME based Epics subsystems provide the controls to the relay switches mounted on the LOS Coil Driver board that engage the control current originated from the front-end subsystems.

l1susauxl0	->	RM,BS,ITMX and ITMY
l1iscauxex	->	ETMX
l1iscauxey	->	ETMY