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 Laser Interferometer Gravitational Wave Observatory (LIGO) Project

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## ISCT1 LAYOUT AND REFL SIGNAL PATH

### Summary:

This is a proposal to increase the light level used to detect the common arm length error signal. We propose to operate with 2 photodetectors in reflection: one for locking and one for running. The option to use the non-resonant sideband (NRSB) for the run-mode detector is presented.

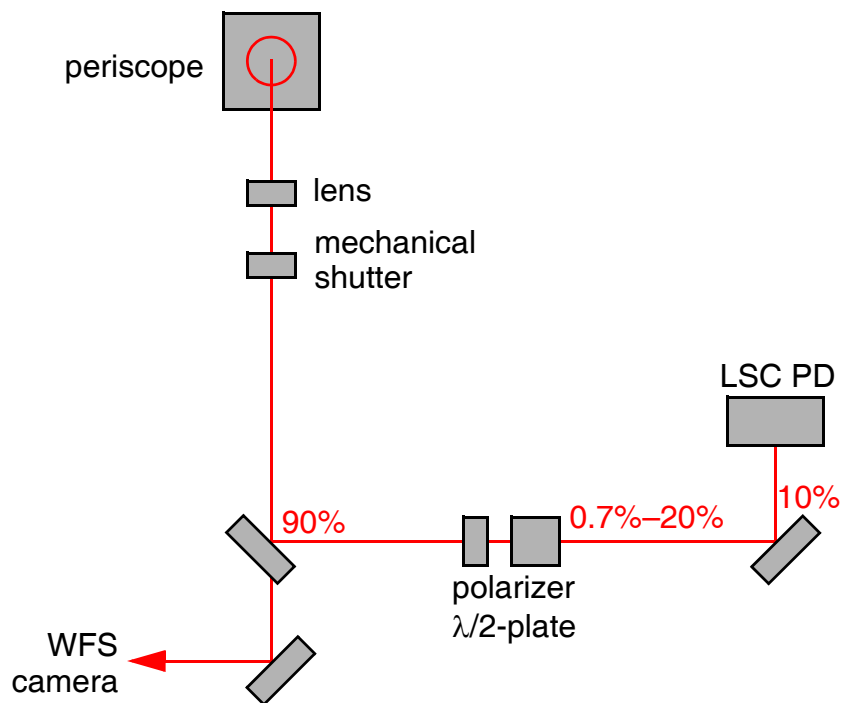
Due to the large increase in gain and light level between locking and running, multiple steps are required to get into run mode: (i) the interferometer is locked with approximately 1 W of input power and with very little light (a few times  $10^{-4}$ ) on the reflection photodetector, (ii) the common mode controls are changed to feed back to the mode cleaner and laser, and the light on the reflection photodetector is increased by about a factor of 30 to approximately 2% using the remote-controlled halfwave plate, (iii) the error signal is switched from the acquisition photodetector to the run-mode photodetector increasing the light level by another factor of 10–50, and (iv) the laser power into the interferometer is increased to its final value.

### Current State:

Figure 1 presents the current layout of ISCT1. During acquisition the fractional power at the LSC photodetector is only  $6 \times 10^{-4}$  (elogs from 9/27/03 and 10/2/03) whereas during running it is about  $2 \times 10^{-2}$ . Figure 2 shows the power on the reflection photodetector while switching the common mode feedback to the mode cleaner and laser. Due to a calibration error in the PREF signal the zero levels are different between high and low power mode (neither of them at zero). Similarly, the gain is a factor of 1.47 too low. The PREF signal is scaled by the input power. Table 1 shows the measured power levels as well as the corrected ones.

**Table 1: Measured power levels on the H1 reflection photodetector.**

State	measured	corrected
low power zero	0.58	0.00
unlocked	1.33	1.1
acquired and locked	0.608	0.041
power increase x30	1.6	1.5
high power zero	0.22	0.00
run mode	0.78	0.82
run mode scaled /30	—	0.027



**Figure 1: Schematic view of current H1 ISCT1 layout.**



**Figure 2: Power in reflection while switching the common mode servo.**

The above table shows that the power indeed increases by about a factor of 30 on the reflection photodetector during the switch of the common mode feedback—as one would expect from the settings of the halfwave plate that changed from 0.007 to 0.2. The power decreases to about 4.5% when the interferometer acquires lock. In run mode it decreases even further to about 2.5% after the QPDX offsets have been adjusted. The sideband power for a modulation depth of  $\Gamma = 0.3$  is about 4.5%. From the above numbers one can conclude that the mode matching of the carrier is fairly good—the amount of light that does not couple into the interferometer is no larger than 2.5%.

Only about 55% of the light that is sent into the mode cleaner appears on the reflection port, if the interferometer is out of lock (see elog from 9/27/03). Together with the measured power ratios from Table 1 one can estimate the absolute power levels at the reflection port.

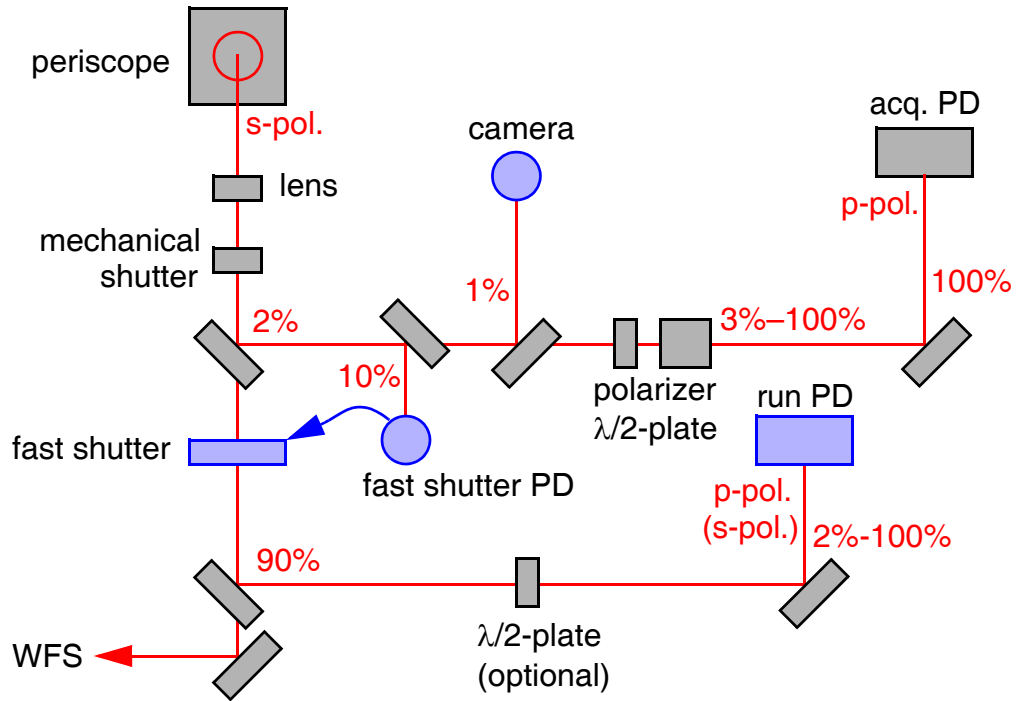
**Table 2: Absolute power level at the H1 reflection port.**

State	MC input power	refl. port power
unlocked	1 W	550 mW
locked	1 W	< 50 mW
run mode	2.5 W	40 mW
run mode	8 W	120 mW

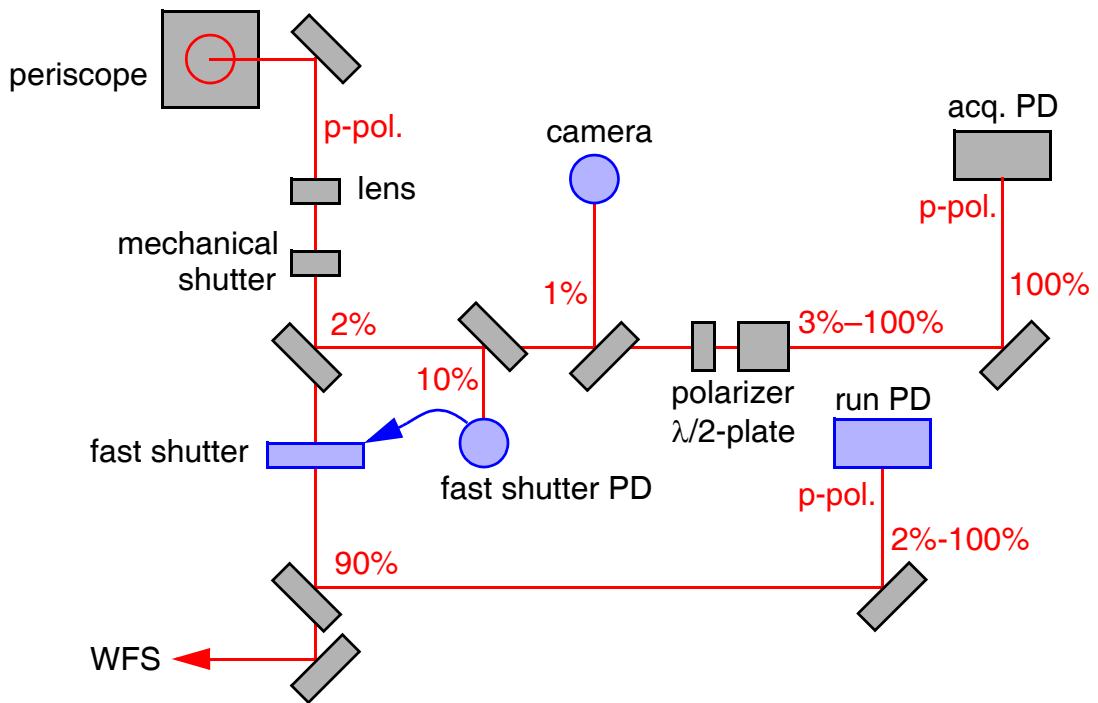
Since the reflection port photodetector uses only about 2% of the light in the current setup, the actual power levels are extremely low with less than a 1 mW of detected light. Increasing the power level with the current setup significantly is not possible without a fast mechanical shutter that automatically closes, when the interferometer falls out of lock.

**Proposed Layout:**

Figure 3 presents the proposed new layout of ISCT1. There is now an acquisition path that splits off 2% of the light. Most of this light is guided to the acquisition photodetector through the polarizer and the halfwave plate. Some fraction of it is split between the camera and a photodetector for the fast mechanical shutter. The main path now incorporates the fast mechanical shutter that protects the wavefront sensors and the run-mode photodetector against the high power when the system is out of lock. Most of the light is available at the run-mode photodetector. The polarizer and the halfwave plate have been kept in the acquisition path to reproduce the current behavior and to avoid adding excess electronics noise to the additive-offset path during the transition to common mode. All optics in the main path are 2". This new layout will use s-polarized light on the run-mode detector unless an additional halfwave plate is installed. This has only a small effect, since the reflection coefficients are similar for both polarizations when operating near 10 degree incident angle (see T980068, pg. 20). An alternate layout that uses p-polarized light all the way and avoids the halfwave plate is shown in Figure 4.



**Figure 3: Schematic view of proposed new H1 ISCT1 layout.**



**Figure 4: Schematic view of an alternate H1 ISCT1 layout using p-polarized light.**

### Non-resonant sideband option:

Using a separate run photodetector makes it possible to use the NRSB. This has several advantages:

- the non-resonant sidebands do not enter the power recycling cavity and should therefore have a well defined spatial mode,
- the orthogonal signal (REFL\_Q) should be small even at high power, and
- the signal strength does not change as function of the sideband power build-up in the power recycling cavity.

There should be no loss in signal-to-noise, if the modulation depth for the NRSB is set to 0.1 and if the main sidebands reach their design throughput to the anti-symmetric port. A disadvantage is that the photodetector has to operate at 62MHz and may have to be reduced in size. There will also be some remaining dependency on the resonant sidebands because of the intermodulation products.

### Electronics:

Figure 5 shows the LSC signals in reflection (REFL\_I and REFL\_Q) as well as the arm powers and the fractional power set with the halfwave plate during a transition into common mode followed by a power-up. The maximum signal level in REFL\_I is about 150 counts to start, it peaks to about 450 during the transition into common mode and settles close to 50 counts. During power-up it again increases to 150 counts. During the same period the maximum of the orthogonal signal (REFL\_Q) grows to approximately 1500 counts. The whitening gain is 21dB, the digital gain is 1.00 and the common gain on the CM board is increased from 0dB to 12dB during the transition into common mode. Table 3 shows the maximum voltage levels at the mixer outputs.

**Table 3: Maximum signal levels at the mixer outputs.**

State	Signal	Max. Voltage	Signal	Max. Voltage
acquired locked	REFL_I	2 mV	REFL_Q	0.1 mV
transition	REFL_I	<10 mV	REFL_Q	
common mode	REFL_I	0.3 mV	REFL_Q	3 mV
power up	REFL_I	1 mV	REFL_Q	20 mV

The fractional power to the LSC photodetector is increased by a about a factor of 30 during the common mode transition and the total input power is increased by 3 during the power-up.

If one would switch from the acquisition photodetector to the run-mode photodetector before the common mode transition, the run-mode detector needs to handle a factor of 30 higher signal levels. This is just about possible with the maximum level at the mixer output reaching 300 mV during transition. With a cable loss of 4dB, a mixer insertion loss of 6 dB and a power splitter loss of 3dB, the signal at the photodetector output is about a factor of 4.5 higher than at the mixer output. The transition peak is most likely due the resonant gain filters in the mode cleaner length servo that get turned off. One may be able to eliminate it by adding resonant gain filters to the common arm cavity path instead. Since this transient happens during the transition of the common mode feedback from the arm cavities to the mode cleaner, but before the additive offset is turned

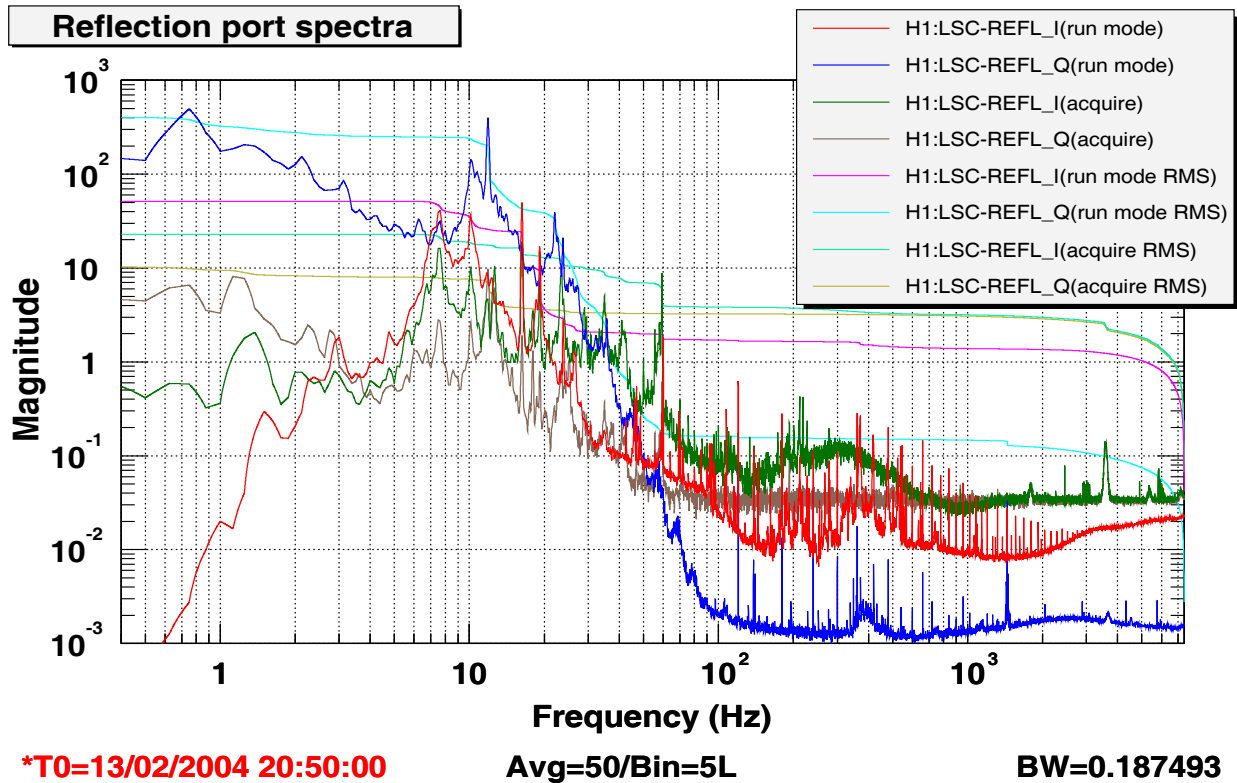
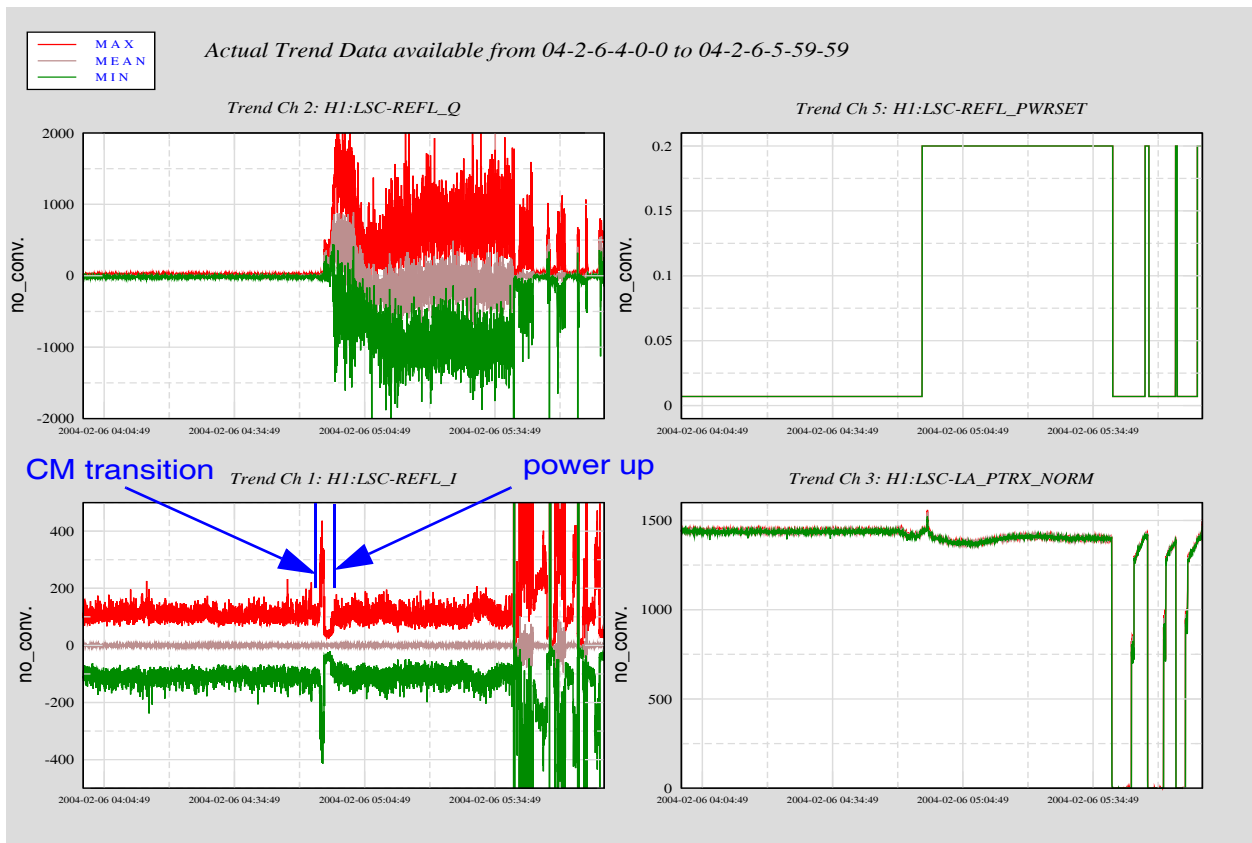


Figure 5: REFL signals. The top graph was measured during a transition into common mode. The bottom graph shows a PSD after acquiring lock and when in run mode.

on, one could also imagine to switch from the acquire to the run mode photodetector at just this time. If this works as expected, the power on the run mode detector before saturation could be as high as 20% of the total light in reflection.

To detect an even higher light ratio one has to switch into full common mode first—thus requiring a new common mode servo board which can switch the analog path between the acquire and the run mode detectors. In this case it is also a good idea to keep the polarizer and the halfwave plate in the acquisition path, so that the contribution of the dark noise decreases during the switch into common mode. A block diagram of a new common mode board is shown in Figure 6.

Features include:

- Switchable inputs for two photodetectors: REFL1\_I\_IN (acquisition mode) and REFL2\_I\_IN (run mode).
- Individually adjustable input gains (−20dB to +20dB).
- Output for digital LSC: REFL1\_I\_OUT (common arm cavity and mode cleaner feedback).
- Selectable input monitor to look at the out-of-loop photodetector: REFL2\_I\_OUT.
- Selectable boost stage in the common path with a pole-zero pair at 50Hz/5kHz and optionally near 10Hz/200Hz.
- Switchable additive offset path.
- Adjustable gain in the additive offset path (−20dB to +20dB).
- Selectable polarity of the additive offset path.
- High pass filter in the additive offset path.
- Open loop measurement capability with an excitation input as well as before and after monitors; available in the common path and in the additive offset path.
- All inputs are differentially sensed; all outputs are driven single ended.
- Data acquisition channel for the additive offset path.

Going beyond the current 2% light ratio will either require that the REFL\_Q signal will be electronically subtracted from the photodiode using feedback controls very much the same as in the AS\_I path, or that we will work with the non-resonant sidebands.

We propose to first implement the simple solution that does not require the new common mode board and to consider the option of the new board only, if it turns out that an intermediate step in common mode with reduced power is necessary or if significantly more light is needed on the run mode photodetector.

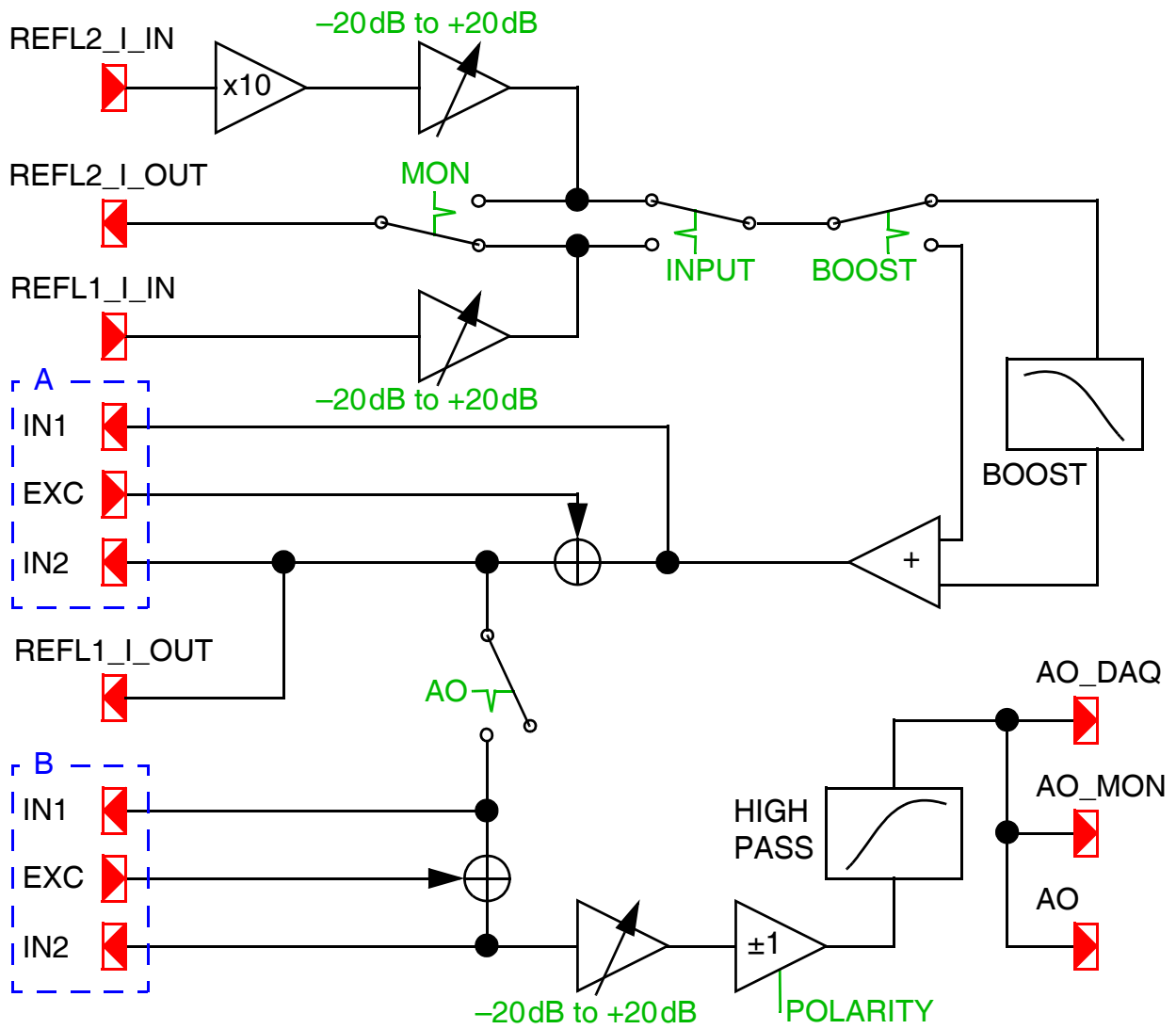


Figure 6: Block diagram of the new common mode board.