LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
CALIFORNIA INSTITUTE OF TECHNOLOGY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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L-BUS PROPOSAL

Paul Schwinberg, Daniel Sigg

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LIGO Hanford Observatory
P.O. Box 159
Richland, WA 99352
Phone (509) 372-8106
FAX (509) 372-8137
E-mail: info@ligo.caltech.edu

LIGO Livingston Observatory
19100 LIGO Lane
Livingston, LA 70754
Phone (504) 686-3100
FAX (504) 686-7189
E-mail: info@ligo.caltech.edu

California Institute of Technology
LIGO Project - MS 51-33
Pasadena CA 91125
Phone (626) 395-2129
Fax (626) 304-9834
E-mail: info@ligo.caltech.edu

Massachusetts Institute of Technology
LIGO Project - MS NW17-161
Cambridge, MA 01239
Phone (617) 253-4824
Fax (617) 253-7014
E-mail: info@ligo.mit.edu

Table of Contents

1 Introduction and Overview

This is a proposal to develop a digital bus for the slow controls of the LIGO interferometers which will eliminate the current “cross-connects”. It is the hope that this will avoid the current noise and EMI problems associated with long cable runs and the potential ground loops. The proposal introduces a digital bus that can operate in a low noise environment and that can be controlled remotely using the familiar EPICS tools. It also introduces analog signals on the backplane that are used for EPICS readbacks and that are used to apply control voltages. The proposal addresses the problem of power distribution by introducing linear post-regulation at the crate and board level. The main goals are to increase modularity, to make modifications and improvements easier by simplifying the wiring, to significantly reduce the number of connections between the digital and analog crates, to increase reliability and maintainability, and to reduced the documentation headaches associated with the historically grown EPICS hardware. The development of this new infrastructure will hopefully also be useful for designing and building advanced LIGO. A migration path is provided for old hardware.

2 The Current Situation

2.1 The Cross-Connects

Most analog boards interface the control system using a VME based EPICS system consisting of digital and analog IO cards. Their signals are routed from the IO boards to the analog boards through a cross-connect. This typically introduces a huge number of connections between the digital and analog crates. Furthermore, it is not a very efficient way to transfer digital data since every bit requires its own electrical wire. The digital IO is optically isolated but the analog connections require a common ground even if differential signalling is used.

2.2 Interfacing Analog Boards

Most analog boards are developed using the eurocard format. They are situated in a eurocard crate and interface to the cross-connect through the P1 connector. More often than not, these lines are not buffered near the connector and noise can be propagated into the board. The connections to other boards typically use connectors on the front panel, whereas the DAQ channels are sent through the P2 connector to the generic DAQ interface board. Again, the connections through the P2 connector seem to be rather noisy for the requirements of the data acquisition system.

2.3 Power Distribution

The eurocard boards are powered through the P1 connector from a central power distribution crate using linear power supplies. Due to the long cable runs and large loads the power near the crates can vary. This is particular true for the +5V supply which can no longer be trusted to be close to specification. An additional disadvantage is that different subsystems are no longer truly isolated from each other, since they are all connected to the same power supply line without true isolation.

3 BASIC FEATURES

3.1 GOALS

The basic goal of this proposal is to provide a new interface for the slow controls. This includes binary inputs and outputs as well as analog inputs and outputs. In detail it should:

i) Operate in a low noise environment and interface with circuits where low noise design is paramount.
ii) Preserve the familiar EPICS interface.
iii) Eliminate the cross-connects.
iv) Provide a modern bus based architecture that uses buffered address and data lines.
v) Replace the analog control lines by A/D and D/A converters in the front-end.
vi) Reduce the interface to the host computer to a single fiber pair.
vii) Provide a migration path from the current situation.

3.2 HARDWARE REQUIREMENTS

We divide the design into a front-end, a host computer and the host computer interface (see Figure 1). The front-end contains the front-side bus (the L-bus), the bus controller and the user boards. The host computer is located in the digital domain and implements the interface to EPICS. The host computer interface is the link between the host computer and the front-end.

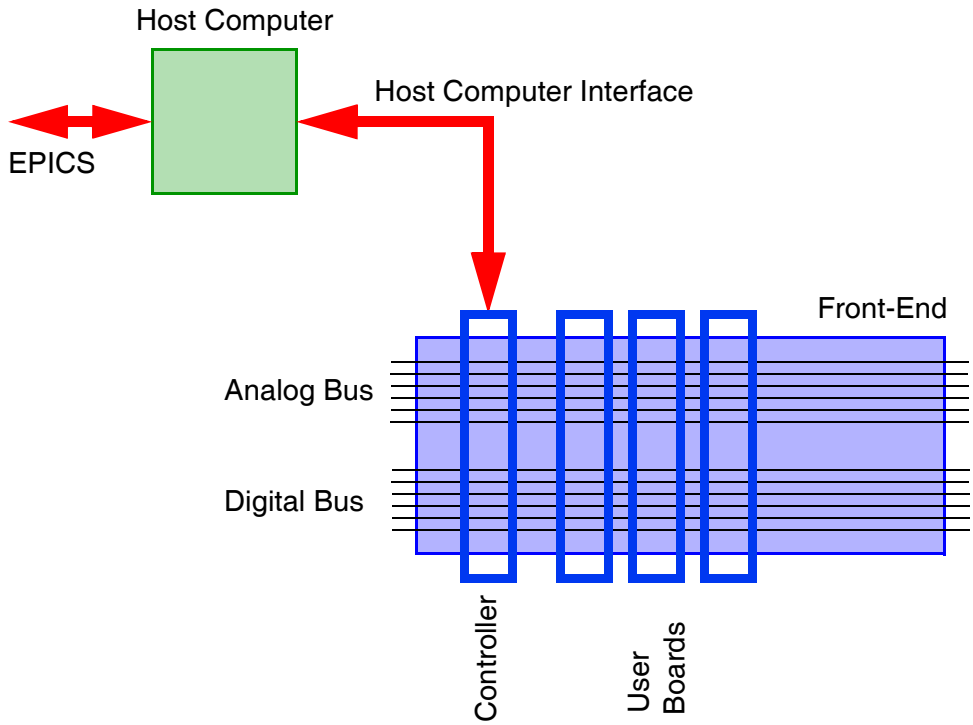


Figure 1: Basic Layout: Eurocard based front-end with L-bus, host computer with EPICS interface and host computer interface.

3.2.1 Front-End Requirements

The front-end needs to support both analog and digital inputs and outputs. The digital interface shall be a memory mapped bused architecture. The analog interface is similar in that it supports dedicated analog lines that get sampled by the bus controller to keep the user boards as simple as possible. The analog readbacks shall support multiplexing to allow for multiple channels per board without a wide bus.

3.2.1.1 General

The general requirements are:

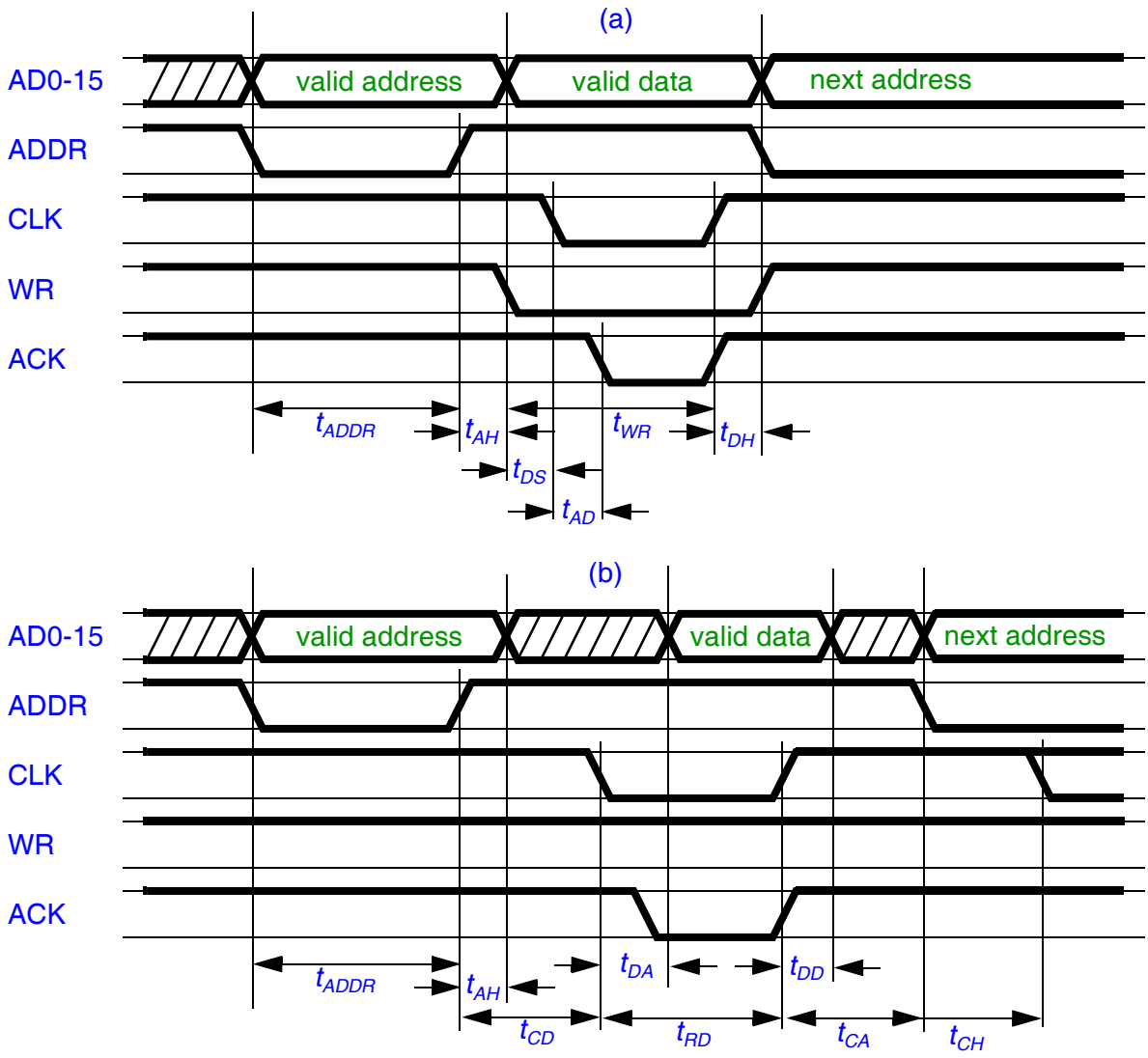
i) A straight forward simple design.
ii) A low noise design without any sharp signal edges.
iii) A memory mapped bus.
iv) Support for multiplexed analog readbacks and analog control lines.
v) A synchronized clock.
vi) Supported physical form factors: eurocrate, stand-alone chassis, field module and migration modules for current eurocard boards.
vii) Detection of not initialized boards.
viii) Standard PCB/Protel building blocks for user boards.
ix) A means to diagnose the bus and to test the functionality of the front-end.

3.2.1.2 Digital Bus

The digital bus shall be implemented on the P2 connector of a eurocrate. Its specifications are:

i) A 16 bit address space. A board is required to decode the top 8 bits and compare it against the board address. Boards that need more than 256 byte of address space can reduce the number of bits used to decode the board address accordingly.
ii) A multiplexed 16 bit address and data bus. Since the word size is 16 bits, the least significant bit of the address is always zero.
iii) A maximum data rate greater than 10kB/s.
iv) A bus fan-out of at least 15.
v) Can be turned off, so that there is no bus activity when not in use.
vi) Implements fully bidirectional buffered bus drivers. Every writable datum can be read back.
vii) Address select (ADDR), write (WR), clock (CLK) and acknowledge (ACK).
viii) An error (ERR) line to indicate that a board needs to be initialized. This is an open-collector line that has to be pulled down to indicate an error. Every user board that implements registers, i.e. uses the digital bus, is required to indicate an error upon power-up. This guarantees that the controller is notified and reloads all necessary values. The line is latched at the controller.
ix) A reset line (RESET) that indicates a master reset. This line is pulled down by the controller when the reset button is pressed. Most analog board will be able to ignore this line.

Figure 2 shows timing diagrams for typical bus read and writes. The bus is deliberately made slow and all user boards are required to be able to read form the bus and write to it in the allowed time. The acknowledge signal can not be used to add a wait but is intended to indicate to the controller that a bus request has been successfully decoded.



Quantity	Description	Typ.	Min.	Max.	Unit
t_{ADDR}	*minimum address clock width*	200	200	—	ns
t_{AH}	*address hold after* ↑ *ADDR*	50	50	—	ns
t_{DS}	*data/WR setup time before* ↓ *CLK*	50	50	—	ns
t_{AD}	*acknowledge after* ↓ *CLK*	20	0	50	ns
t_{WR}/t_{RD}	*minimum data clock width*	200	200	—	ns
t_{DH}	*data/WR hold after* ↑ *CLK*	50	50	—	ns
t_{CD}	*clock delay after* ↑ *ADDR*	50	50	—	ns
t_{DA}	*maximum data access time*	—	0	100	ns
t_{DD}	*maximum data delay after* ↑ *CLK*	0	0	50	ns
t_{CA}	*next address clock after* ↑ *CLK*	—	50	—	ns
t_{CH}	*minimum clock high state*	—	100	—	ns

Figure 2: Timing diagrams for a bus write (a) and a bus read (b).

3.2.1.3 Analog Bus

There are basically two ways to implement analog readbacks and control lines: The ADCs and DACs can be implemented on the user board and are read and written through the digital interface. For control lines this is the preferred solution. Since most analog boards require analog channels at slow rate for at least some channels, the controller provides its own set of ADCs and DACs. This support is limited to keep the number of analog lines on the backplane low. However, the analog readback lines can be multiplexed using a separate address that is cycled through fully at 16Hz by the controller. The analog lines shall use the P2 connector. Its specifications are:

i) 4 bits of address for multiplexing the analog readbacks.
ii) Up to 16 lines for analog readbacks. The idea is that each board uses up a single line and multiplexes its analog readback channels onto it by decoding the 4 bit address. A user board can assume that one of these lines is available for its use.
iii) Up to 8 lines of analog control signals. Only boards that use control signals that need constant updating during operations should have the option to use these lines rather than an on-board DAC. A user board cannot assume that one of these lines is available, but must provide an on-board DAC that can be jumped out in favor of one of these lines.

Table 1 shows the recommended number of supported analog readback and control signals for different chassis and crate configurations.

Table 1: Number of supported analog channels.

Format	eurocrate with full width backplane 21 slots	eurocrate with half width backplane 10 slots	stand-alone chassis 1U or 2U height 1–2 slots
Number of analog readbacks	16	8	2
Number of analog control signals	8	8	4

3.2.1.4 Power Supply Requirements

DC power is provided from a central location. The supplied voltages are ±10V and ±24V. To guarantee good voltages and to isolate the front-ends from one another, linear post regulation is provided. The specifications are:

i) Supported voltages: +5V (digital), ±5V (analog), ±15V, ±24V (raw).
i) The maximum current allowed per board is 1A for each 5V supply and 500mA for each 15V power supply. A maximum of 1A applies for the unregulated 24V supplies.
ii) Linear post regulation for the ±5V and ±15V supplies are provided to all boards within a eurocrate or stand-alone chassis. The ±24V supplies are provided in raw format and can be used for on-board regulation where required.
iii) Passive cooling system where possible; duct air where needed.
iv) On-board regulation is allowed for critical systems.
v) All voltages are monitored and failures are reported to the controller (using the ERR line). The specifications are between 4.75V and 5.25V for the 5V supplies and between 14.25V and 15.75V for the 15V supplies, respectively. The unregulated supplies are specified to be within 9V and 12V and to be within 22V and 28V, respectively.
vi) An on/off switch.

Table 2: List of signal and power lines.

Line	Description	Type	Conn./Pin	
$\overline{\text{RESET}}$	Master reset on crate	Digital	P2	1A
$\overline{\text{ERR}}$	Indicates an error	Digital	P2	2A
$\overline{\text{ADDR}}$	Address is valid	Digital	P2	3A
$\overline{\text{WR}}$	Data direction is write	Digital	P2	4A
CLK	Datum needs to be returned by board	Digital	P2	5A
$\overline{\text{ACK}}$	Datum is valid (when board is ready to be read)	Digital	P2	6A
N/A	reserved, currently not used	Digital	P2	7A/8A
VCC	+5V for digital circuits	Power	P2	9A-16A
AD0–AD7	Address and data lines, LSB	Digital	P2	17A–24A
AD8-AD15	Address and data lines, MSB	Digital	P2	25A–32A
DGND	Return ground for digital bus	Power	P2	1B–32B
N/A	Not bused, available on a back connector	User	P2	1C–32C
ADCp0–ADCp15	Analog readbacks, positive	Analog	P1	1A–16A
ADCn0–ADCn15	Analog readbacks, negative	Analog	P1	1C–16C
AA0–AA3	Address of analog readbacks	Analog	P1	19A–22A
DACp0–DACp7	Analog control signals, positive	Analog	P1	25A–32A
DACn0–DACn7	Analog control signals, negative	Analog	P1	25C–32C
N/A	bused, currently not used	Analog	P1	17C–24C
reserved	+LV power supply	Power	P1	1B/2B
reserved	–LV power supply	Power	P1	5B/6B
+5V	+5V power supply (post regulated)	Power	P1	9B/10B
–5V	–5V power supply (post regulated)	Power	P1	13B/14B
+15V	+15V power supply (post regulated)	Power	P1	17B/18B
–15V	–15V power supply (post regulated)	Power	P1	21B/22B
+24V	+24V power supply (raw)	Power	P1	25B/26B
–24V	–24V power supply (raw)	Power	P1	29B/30B
AGND	Analog ground	Power	P1	17A/18A 23A/24A 3B/4B 7B/8B 11B/12B 15B/16B 19B/20B 23B/24B 27B/28B 31B/32B

3.2.1.5 Physical Size

The selected eurocard format is 6U (223 mm) × 220 mm. This gives about 40% more real estate than the currently used boards (223 mm × 160 mm) and should be sufficient to accommodate the additional bus logic and data converters.

The supported chassis and crate configurations are:

i) Eurocrate: Option 1 is a full width backplane. This supports 21 slots including the one used for the controller. Option 2 is one or two half width backplanes with 10 slots each.

ii) Stand-alone chassis: Either a 1U or 2U high 19" rack mountable chassis. The controller is mounted in the back. One or two slots for user boards are provided.

Figure 3 shows a possible crate from AWG/Electronics Solutions (959-267637C) that is enclosed on all sides. This type of crate provides shielding against EMI provided that the user boards implement proper feed-through for their front-panel connectors and that the empty slots are covered. The dimensions of the crate are 6U × 84HP × 360 mm. This leaves about 100 mm in the back to install the power supplies. Heat sinks are mounted on the outside of the back panel, whereas the linear voltage regulators are mounted on the inside. The dc power is connected through the back panel using proper EMI filtering.

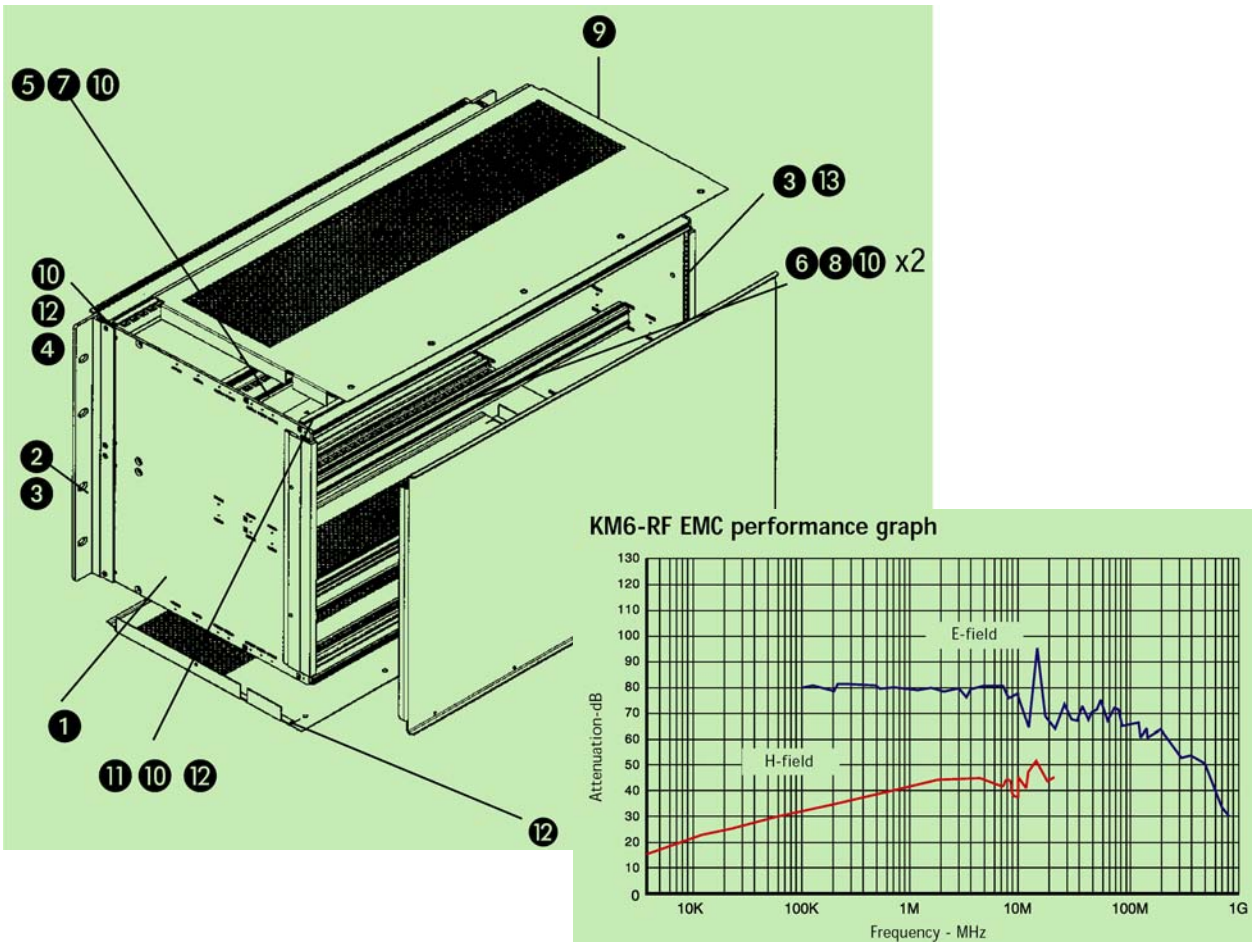


Figure 3: APW/Electronic Solution crate with EMC panels.

3.2.1.6 Migration Path

The increase in physical size makes it possible to develop a 223 mm×60 mm adapter boards that fits between the L-bus and the older boards. This adapter board would include 16–32 binary outputs and 16 binary inputs that can be wired to any P1/P2 connector pin of an old board. Similarly, it would provide a mux for 16 analog readback channels that again can be wired to any P1/P2 connector of an old board. Optionally, one should be able to add up to 8 digital-to-analog converters for digital control lines. Most currently built boards would be covered by this adapter board (see Appendix A). In some situations it might be preferable to make a new layout of an old board with the new interface integrated.

In the current setup some of the DAQ channels are routed through the backplane. This is no longer supported for new designs where DAQ channels should use standard front-panel connectors. Legacy boards should be updated to do the same—or if not feasible, they can use the C row on the P2 connector to emulate the old behavior.

It should be mentioned that because in most cases the existing boards don't communicate with one another through the backplane, it is straight forward to convert only part of the existing hardware to the new standard and convert the remainder as time permits.

3.2.2 Host Computer Interface Requirements

The communication between the front-end and the host computer shall be through a serial link. Its requirements are:

i) Point to point bidirectional serial link.
ii) Option for optical fiber connection to minimize EMI problems.
iii) Maximum link length of several 100 m (when using optical fibers).
iv) Support the full data rate of the front-end bus.
v) Some sort of communication protocol to transfer data from the front-end to the host computer.
vi) A stand-by mode that can be invoked to stop all bus activity.

The front-end will also require a timing signal to synchronize the analog readbacks to the GPS clock. A single fiber will provide the clock signal as well as the 1 pps.

3.2.3 Host Computer Requirements

The host computer is responsible to interface the front-end with the control room. Its requirements are:

i) Acts as an EPICS channel server and contains EPICS database records to support the new hardware controls interface.
ii) Support of multiple (fiber) connections to analog front-ends.
iii) Efficient interface to the DAQ system to avoid the EPICS/ethernet bottleneck.
iv) Possibly use a cheaper alternative to the current VME based CPUs.

3.3 Software Requirements

The software running on the host computer needs to communicate with the front-end through the host computer interface and provide the necessary drivers to make the channels available through EPICS. Figure 4 shows a view of the different software layers.

3.3.1 Low Level Hardware Driver

The low level hardware driver basically supports a read and write function. Its arguments are:

i) A crate address which selects the link to a front-end.
ii) An address which will be used to access a user board.
iii) A datum field which can be either in or out depending on the transfer direction.
iv) A return value indicating the success of the IO operation.

The low level hardware driver also has a control function that lets one put the front-end controller into stand-by mode. Preferably, the link is also turned off in this situation.

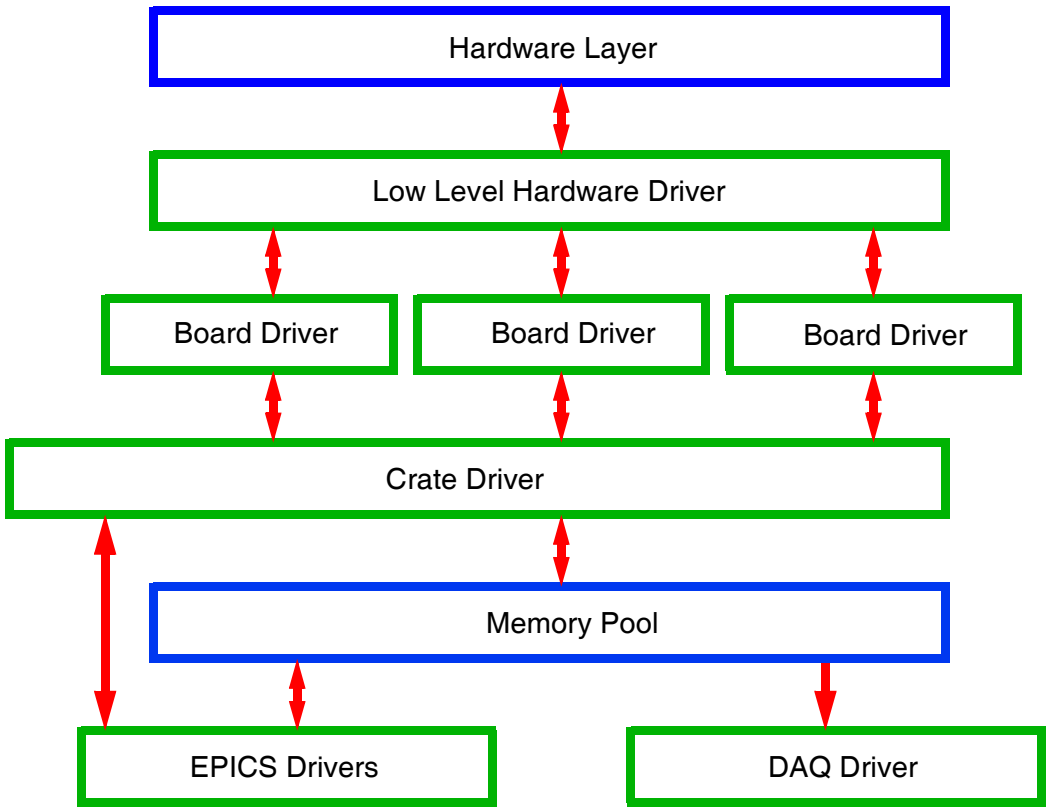


Figure 4: Software Infrastructure.

3.3.2 Board Driver

Most boards will be able to use a generic board driver that can be setup through a configuration file. The board configuration file contains:

i) The board base address, i.e., 0x0400, 0x0500,... 0xFF00. The address range 0x0000 to 0x3FFF is reserved for the crate controller.
ii) A list of analog input channels. Each entry specifies a channel name, its digital bus address or the analog bus address (bus line number and multiplex index), the number of used bits, the engineering units conversion, the limits, the precision and the scan rate.
iii) A list of analog output channels. Each entry uses the same parameters as an analog input channel with the exception of the analog bus address that consist of a bus line number only.
iv) A list of binary input bits. Each entry specifies a channel name, its digital bus address, the word size and the bit index.
v) A list of binary output bits. The parameters are the same as for a binary input channel.

A board configuration file is specific to a board and can be used to generate the EPICS database.

3.3.3 Crate Driver

The crate driver is a background task that is used to communicate with the front-end. It has functions to talk to the crate controller and knows about the installed boards from the crate configuration file. The crate configuration file contains:

i) The crate address which specifies the link.
ii) The crate name which is used in the user interface.
iii) The version of the crate controller.
iv) A list of board drivers with associated configuration files. This list should correspond to the set of installed user boards.

3.3.4 Memory Pool

The crate driver uses a memory pool that contains a list of all channels associated with all crates and boards controlled by this host computer. The memory pool contains the current values of all channels and is used by the DAQ driver as well as the EPICS drivers.

3.3.5 EPICS Drivers

The EPICS drivers interface with the crate driver to write and read values from and to a board, respectively. Since the crate driver writes scanned channels into the memory pool automatically, their value can be obtained directly from there. The EPICS database definitions can be generated automatically from the crate and board configuration files.

3.3.6 DAQ Driver

The DAQ driver reads the memory pool at a rate of 16 Hz. It collects the data in blocks of 16 s before they are send to the frame builders. This direct connection will avoid the high overhead associated with reading single EPICS channels into the DAQ.

4 Design Considerations

4.1 Bus Drivers and Bus Decode Logic

The bus drivers are TTL logic gates. The data and address transceivers on both the controller and the user boards are SN74LS245 chips. The logic lines are buffered on the user board using a SN74LS125. The error line can be pulled down upon power reset with a simple RC-type circuit (see example schematics). In most circumstances the reset line can be ignored. If not, it should be buffered with a SN74LS125 as well. A typical implementation of the digital interface on the user board is shown in the schematics “L-Bus: User Board Example”. To conserve power logic chips on the inside may be selected from one of the TTL-compatible CMOS families (HCT, ACT or FCT).

4.2 Analog Readbacks

The analog readback signals are read back through a multiplexer on the user board so that only a pair of analog lines is used. The multiplexer can be a Maxim MAX306 or an Analog Devices ADG406. The output of the multiplexer is buffered with an OpAmp that has a 100kHz bandwidth. The output of the OpAmp is sent to the positive terminal of the analog readback, whereas the negative one is connected to analog ground with a 50Ω resistor. Unused inputs of the multiplexer are also connected to ground with a 50Ω resistor, so that they can be field modified easily. A typical implementation of the analog readback interface on the user board is shown in the schematics “L-Bus: User Board Example”.

4.3 Analog Control Signals

The analog control signals provided by the controller board use 16 bit digital-to-analog converters such as the AD660BR (8 bit interface) or AD669BR (16 bit interface) from Analog Devices or the DAC712UL (16 bit interface) from Burr-Brown. These analog signals are filtered and buffered before they are put on the analog backplane. Two poles at 20Hz are provides for filtering. This should bring the static output noise of these devices below 10nV/√Hz above 100Hz. These signals are meant for boards that need constant update during operations. This way the bus activity on the digital bus can be avoided. For all other purpose the DAC should be implemented directly on the user board. An example that uses a 16 bit DAC is shown in the schematics “L-Bus: User Board Example”. In this example one can choose whether to use the internal DAC or one of the controller provided DAC signals.

If lower resolution DACs are sufficient, the Burr-Brown DAC7725 is a quad 12 bit converter that can be directly interfaced with the digital bus (see example in “L-Bus: User Board Example”). Another possibility is the Burr-Brown DAC7744 which is a quad 16 bit converter that again can be interfaced directly with the digital bus, but comes in a shrink small outline package.

4.4 Bus Controller

The bus controller has to be able to translate requests from the host computer into a bus access on the digital backplane, into reading one of the muxed analog readbacks or into writing one of the

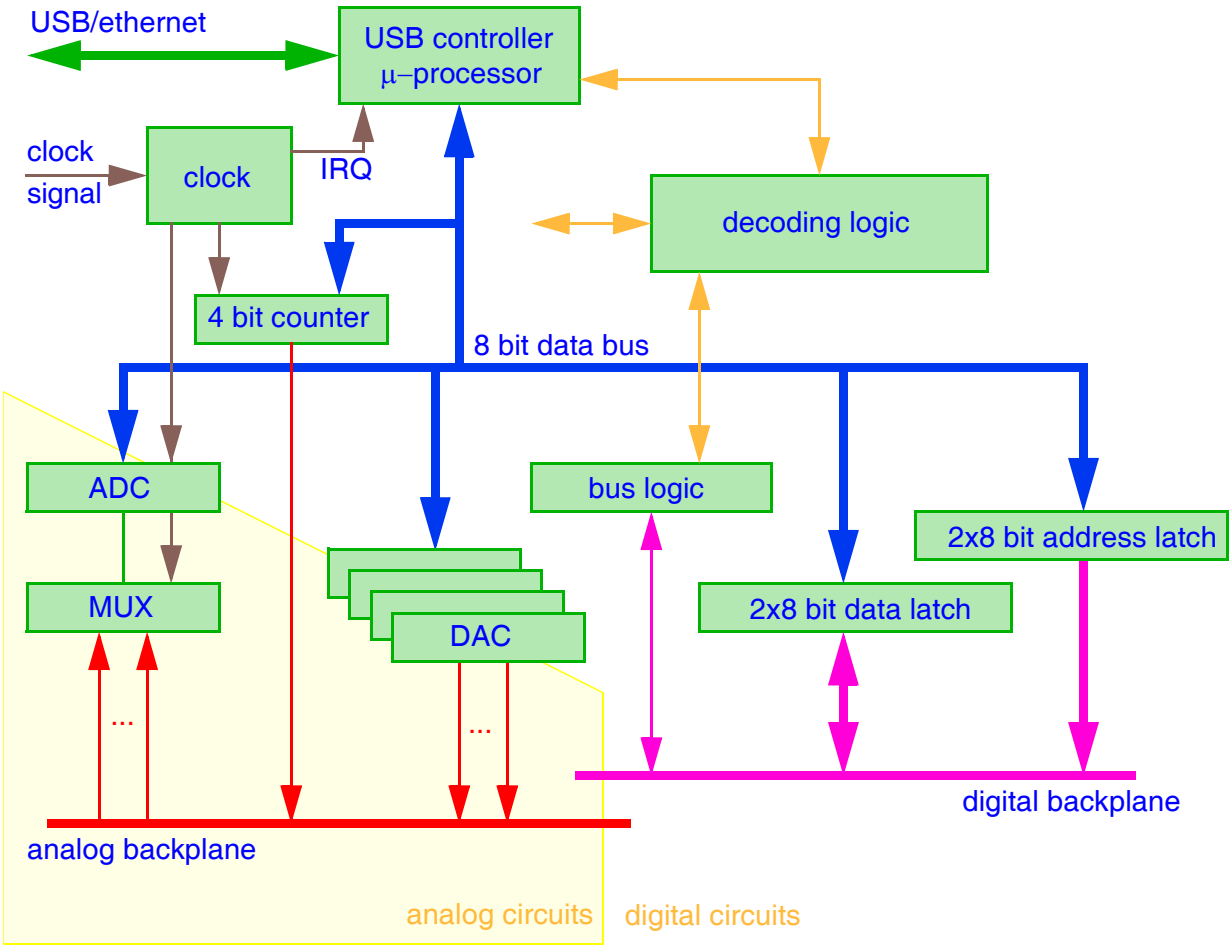


Figure 5: USB or ethernet based bus controller.

analog control signals. It also needs to provide a clock signal to cycle through the analog readback channels and to synchronize the EPICS readback with 16Hz. Figure 5 shows a block diagram of the bus controller. It is controlled by either a USB controller such as the Cypress AN2135SC or a microprocessor with integrated ethernet adapter such as the Zilog EZ80F91. The USB controller will require the controller to be with a couple of meters unless a USB-to-fiber converter is used such as the S.I.TECH 2170/2171. The ethernet base controller would be able to implement a fiber link using the 100base-FX standard.

The other required input is a 2^{24}Hz clock signal with an encoded 1pps which again can be fiber coupled. The board has an internal 2^{24}Hz VCXO that is phase-locked to the clock signal. The clock controls the data rate of the on-board ADC, its multiplexer and the 4 bit analog address that are used to sense the analog readback channels. Since there are a maximum of 256 analog readback channels (16 analog lines multiplexed by 16 each) that are sampled at 16Hz, the ADC runs at 4096 Hz. This clock is also used as a heartbeat for the USB controller/microprocessor.

The USB controller/microprocessor uses an 8 bit bus to load data from the ADC, the 4 bit counter or the digital backplane. It sends data to the DACs and the digital backplane (address and data). A few control lines are used to decode which devices need to response.

APPENDIX A SURVEY OF CURRENT BOARDS

This is a rough estimate on the number of slow channels currently deployed. It is not intended to be an accurate enumeration—rather it is an overview to help sizing the new system.

A.1 PSL AUXILIARY CRATE

Table 3: Signal count for PSL auxiliary crate.

Board	#	binary in	binary out	analog in	analog out
D980352-B: PMC	1	3	0	3	3
D980536-D: FSS	1	5	0	4	6
D980399-B: ISS	1	2	0	2	2
D980353-C: Freq. Ref.	1	1	0	2	1
D980401-A: VCO (stand-alone)	1	2	0	1	1
Total	5	13	0	12	13

A.2 IOO AUXILIARY CRATE

Table 4: Signal count for IOO auxiliary crate.

Board	#	binary in	binary out	analog in	analog out
D00347-B: MC Servo	1	5	13	4	3
Total	1	5	13	4	3

A.3 LSC AUXILIARY CRATE

Table 5: Signal count for IOO auxiliary crate.

Board	#	binary in	binary out	analog in	analog out
D990511-00: Demod	7	0	0	0	3
D990543-01: PD Interface	2	1	1	1	2
ASI (stand-alone)	2	0	0	0	0
D990694-00: Whitening board	3	11	4	8	0
D000076-01: AA board	3	8	0	0	0
D000086-01: CM board	1	4	12	3	6
D020061-A: Eurocard driver board	3	0	0	0	0
Total	21	63	26	29	31

A.4 ASC Auxiliary Crate

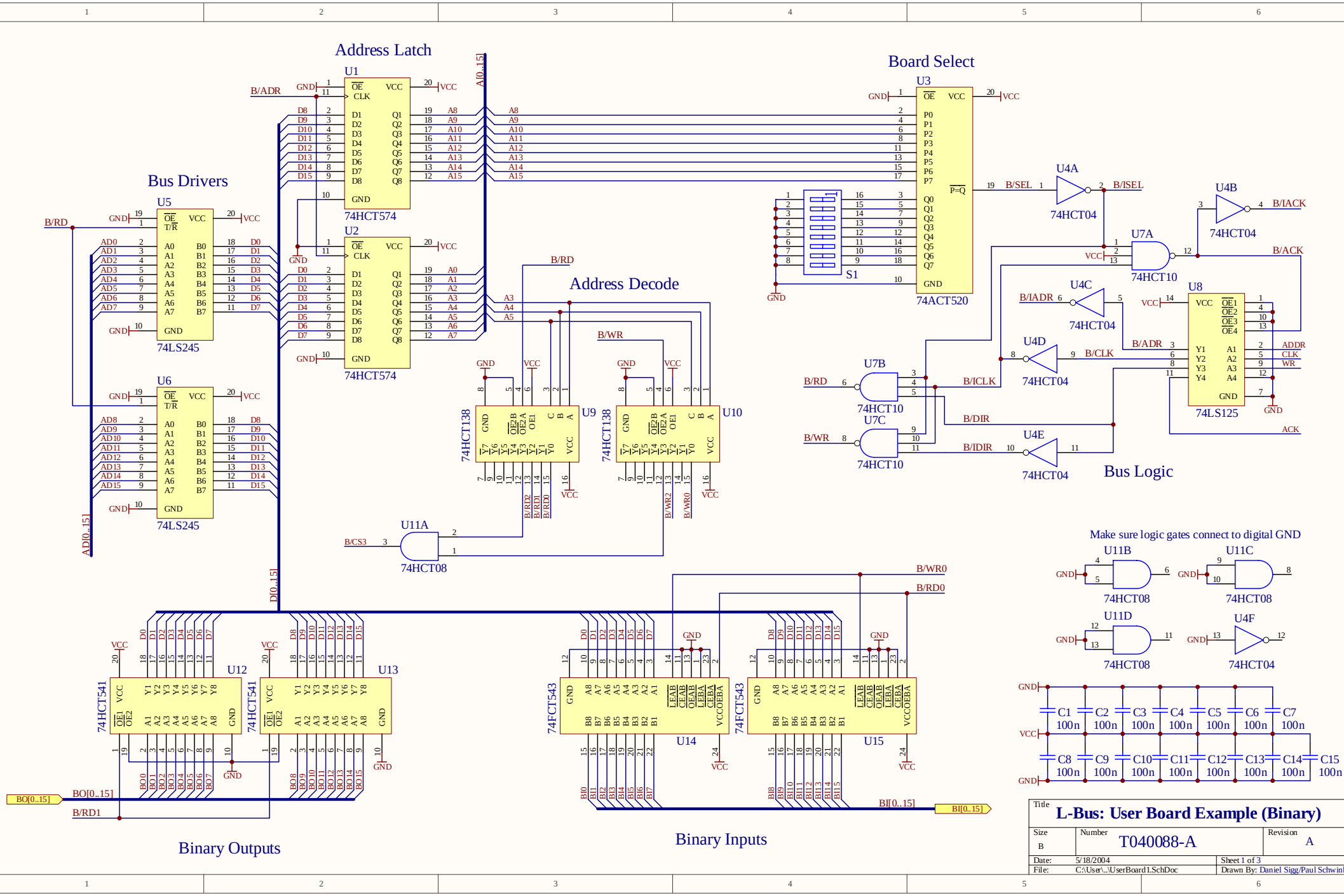
Table 6: Signal count for ASC auxiliary crate.

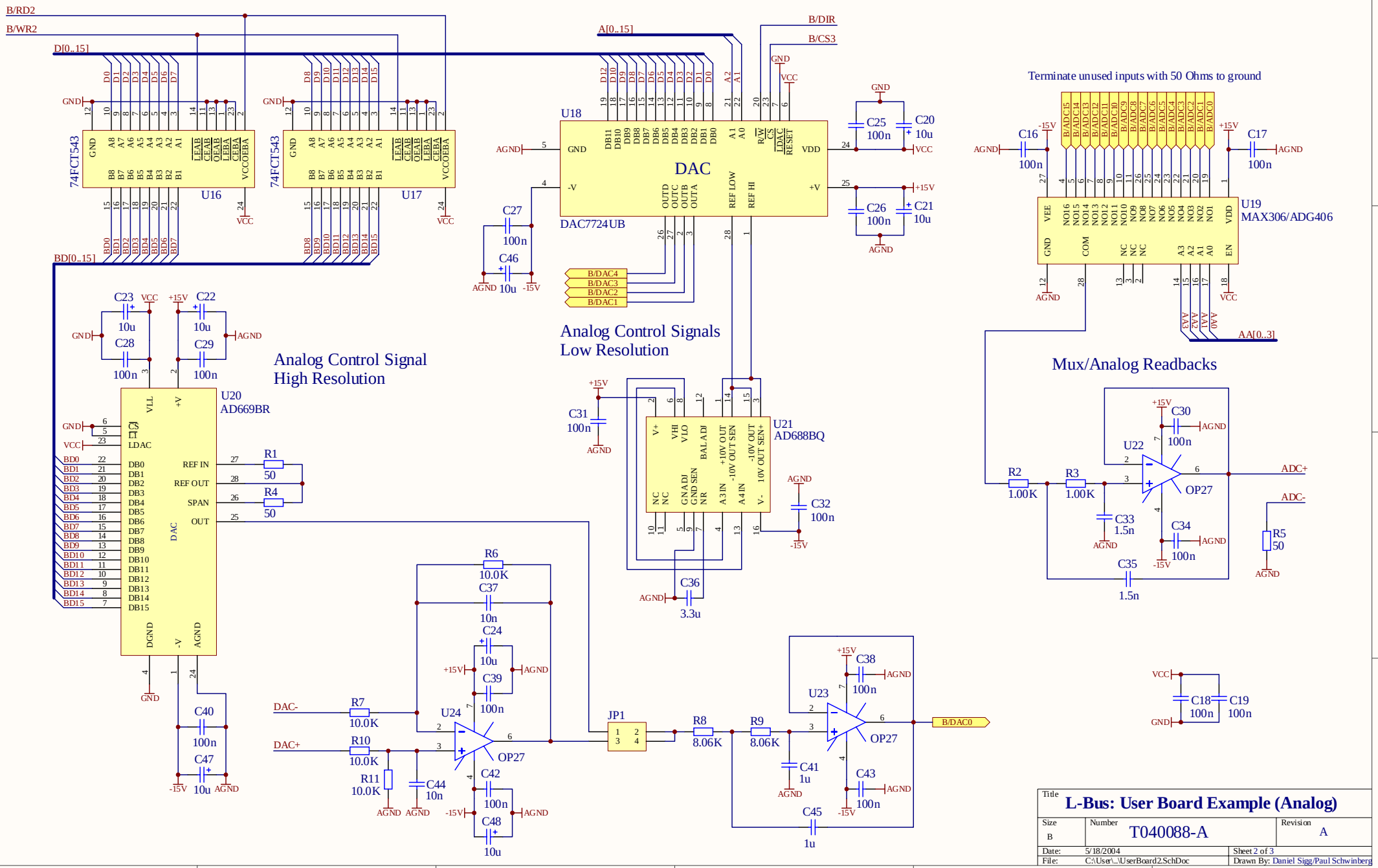
Board	#	binary in	binary out	analog in	analog out
D980233-B: WFS demod	7	8	0	1	13
D990196-B: WFS whitening	7	16	0	8	0
D990195-A: WFS DC whitening	2	0	0	0	0
D980323-C: PZT driver	1	4	0	4	6
Total	1	172	0	67	97

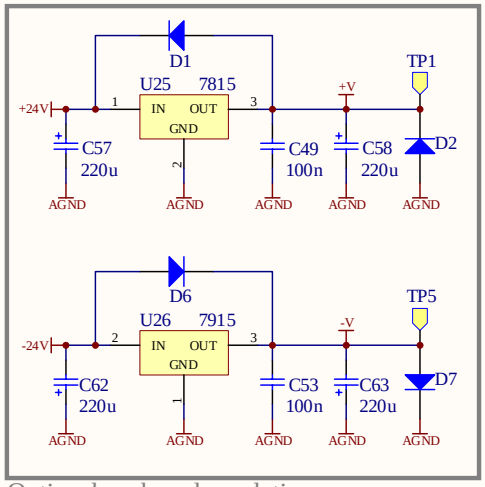
A.5 SUS Auxiliary Crate

Table 7: Signal count for SUS auxiliary crate.

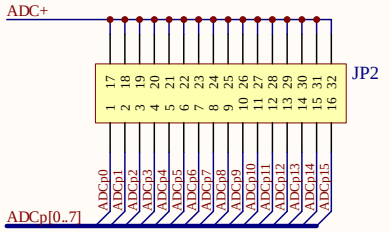
Board	#	binary in	binary out	analog in	analog out
D000325-A: LOS Coil Driver (stand-alone)	6	7	4	0	13
D010001-B: SOS Coil Driver	7	10	0	4	5
D000210-A: SUS PD whitening	13	5	0	0	5
D000316-A: SOS dewhite an AI	5	8	0	0	8
D000186-C: Anti-image	5	0	0	0	8
D000183-C: Dewhite	7	4	0	0	0
D000341-A: LOS Bias Module	6	0	0	4	4
D010284-00: Pole-zero module	1	8	0	0	0
Total	1	253	24	52	282

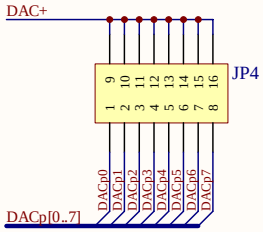

Address Latch
Board Select
Bus Drivers
Address Decode
Bus Logic
Binary Outputs
Binary Inputs
U1
U2
U3
U4A
U4B
U4C
U4D
U4E
U4F
U5
U6
U7A
U7B
U7C
U8
U9
U10
U11A
U11B
U11C
U11D
U12
U13
U14
U15
S1
74HCT574
74ACT520
74HCT04
74HCT10
74LS245
74HCT138
74HCT08
74LS125
74HCT541
74FCT543
B/ADR
B/RD
B/WR
B/CS3
B/ISEL
B/IACK
B/ACK
B/IADR
B/ICLK
B/CLK
B/DIR
B/IDIR
ACK
ADDR
CLK
WR
B/RD2
B/RD1
B/RD0
B/WR2
B/WR0
B/RD0
B/RD1
A[0..15]
D[0..15]
AD[0..15]
BO[0..15]
BI[0..15]
Make sure logic gates connect to digital GND
C1 100n
C2 100n
C3 100n
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
Title
L-Bus: User Board Example (Binary)
Size
B
Number
T040088-A
Revision
A
Date:
5/18/2004
Sheet 1 of 3
File:
C:\User\..\UserBoard1.SchDoc
Drawn By: Daniel Sigg/Paul Schwinberg

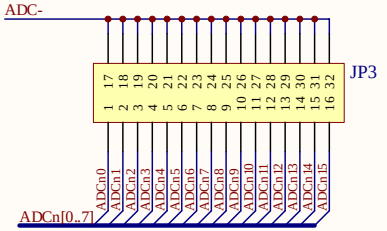

B/RD2
B/WR2
D[0..15]
BD[0..15]
A[0..15]
B/DIR
B/CS3
74FCT543
U16
U17
DAC
DAC7724UB
U18
B/DAC4
B/DAC3
B/DAC2
B/DAC1
Analog Control Signal
High Resolution
U20
AD669BR
Analog Control Signals
Low Resolution
U21
AD688BQ
Terminate unused inputs with 50 Ohms to ground
U19
MAX306/ADG406
AA[0..3]
Mux/Analog Readbacks
U22
OP27
ADC+
ADC-
U24
U23
JP1
B/DAC0
DAC-
DAC+
Title
L-Bus: User Board Example (Analog)
Size
B
Number
T040088-A
Revision
A
Date:
5/18/2004
Sheet 2 of 3
File:
C:\User\..\UserBoard2.SchDoc
Drawn By: Daniel Sigg/Paul Schwinberg

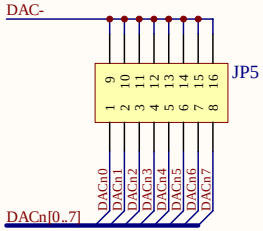


Optional on-board regulation

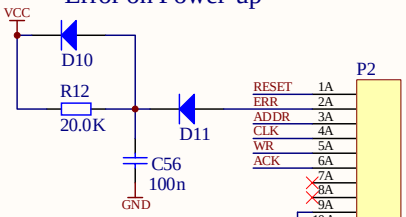








Error on Power-up



Title	L-Bus: User Board Example (Backplane)		
Size: B	Number: T040088-A		Revision: A
Date: 5/18/2004		Sheet 3 of 3	
File: C:\User\...\UserBoard3.SchDoc		Drawn By: Daniel Sigg/Paul Schwinberg	