LIGO Laboratory / LIGO Scientific Collaboration

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Characterization of an Advanced Converter Design

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Abstract

The Laser Interferometer Gravitational-Wave Observatory [LIGO] uses analog-to-digital [ADC] and digital-to-analog [DAC] converters in its sensing and control systems to permit communication between computers and hardware. The upgrade to Advanced LIGO will be more sensitive and requires the use of more converters. The goal of this project is to test a new converter design, which is less expensive and has lower noise levels than the current converters. Comparing the response of the converters to known test signals permits an assessment of the converters' performance. Results so far indicate that the new analog-to-digital converters have significantly lower noise levels than the previous converters. Data gained from this project will be used to determine what changes will need to be made for the final converter design.

Background

LIGO is working to detect gravity-waves, ripples in space-time. However, gravity waves are extremely weak[1], making low-noise sensing and control equipment necessary.

All information sent to and from instruments must pass through a converter. This is because most real world signals are analog. Analog signals may take any value. An analog signal ranging from zero to ten could have a value of zero, ten, or anything in between, like two and a half. However, computers are digital. The values they take are quantized, so that the computer can only receive or send values that are multiples of a certain value. For instance, a simple digital signal ranging from zero to ten might only have values that are integers. Other values, like two and a half, will not be possible for this digital signal. Furthermore, analog signals have a value at every instant. A digital signal to a computer has values only at intervals, such as one every second. The digital signal has no information in the middle of such an interval.

For instance, an analog signal might be the position of a yo-yo. It can have any position between the hand holding it and the full length of its string, and it exists somewhere at every time. A digital signal is like a series of snapshots of the yo-yo next to a ruler. The snapshots are taken at specific intervals; there are no pictures of the yo-yo in between snapshots. The yo-yo is also next to only one mark on the ruler at a time. If it is in between marks, it is assigned one of the two marks next to it. Its position is always a specific mark.

Because of these different requirements for analog and digital systems, converters are needed for data to be transmitted between them. Unfortunately, this conversion process introduces error into the signal, causing noise. Conversion from analog to digital introduces some noise because the digital signal has a limited number of possible values. Both conversions add noise through their physical components. Additionally, circuit boards containing the converters are expensive. About a million dollars have been spent on such converters for LIGO[2].

LIGO is in the process of an upgrade to Advanced LIGO. Advanced LIGO will be far more sensitive. Advanced LIGO will also need roughly three times as many converters[3]. As a result, quieter and less expensive converters are desirable[4].

To this end, a pair of identical test boards has been built. Each test board contains eight channels, four of which convert from analog to digital. The other four convert from digital to analog.

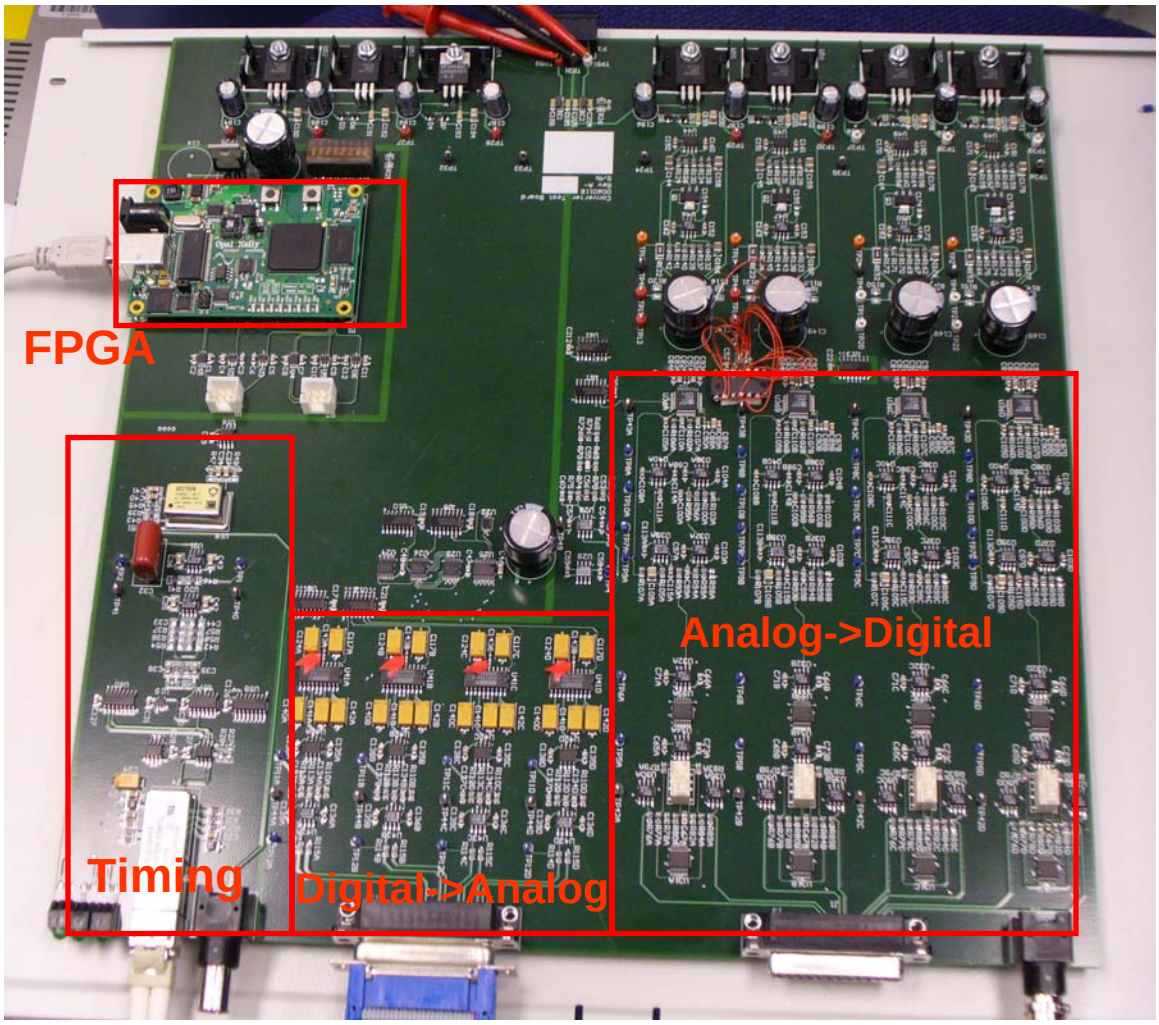

Figure 1 One of the converter test boards.

The boards have a different configuration from previous boards, in addition to different components. They also include a field-programmable gate array, or FPGA. The FPGA allows a computer to communicate with and control the test board. The FPGA is also programmed to include digital logic for manipulating the signals passing to and from the computer.

The purpose of this project is to test the new design and determine how it compares to the converters currently used in LIGO. The main factor being tested is the noise level. The goal is to have the noise below a specific fraction of the maximum possible input or output from the board, for the ADCs and DACs respectively. This is inversely related to the signal-to-noise ratio, which is the magnitude of the signal divided by the magnitude of the noise.

Results so far have been encouraging. The FPGA will communicate with the test boards. Tests have shown that the analog-to-digital conversion has far lower noise levels

than the converters LIGO currently uses. The digital-to-analog converters are also performing close to the desired levels.

ADC

The analog-to-digital conversion was the first to be tested. The test setup inputs an analog sine wave to the board, and reads the digital result on a computer. Then the frequency spectrum of the output is taken and analyzed for at frequencies away from the sine wave at the input. A notch filter was used to significantly reduce the magnitude of

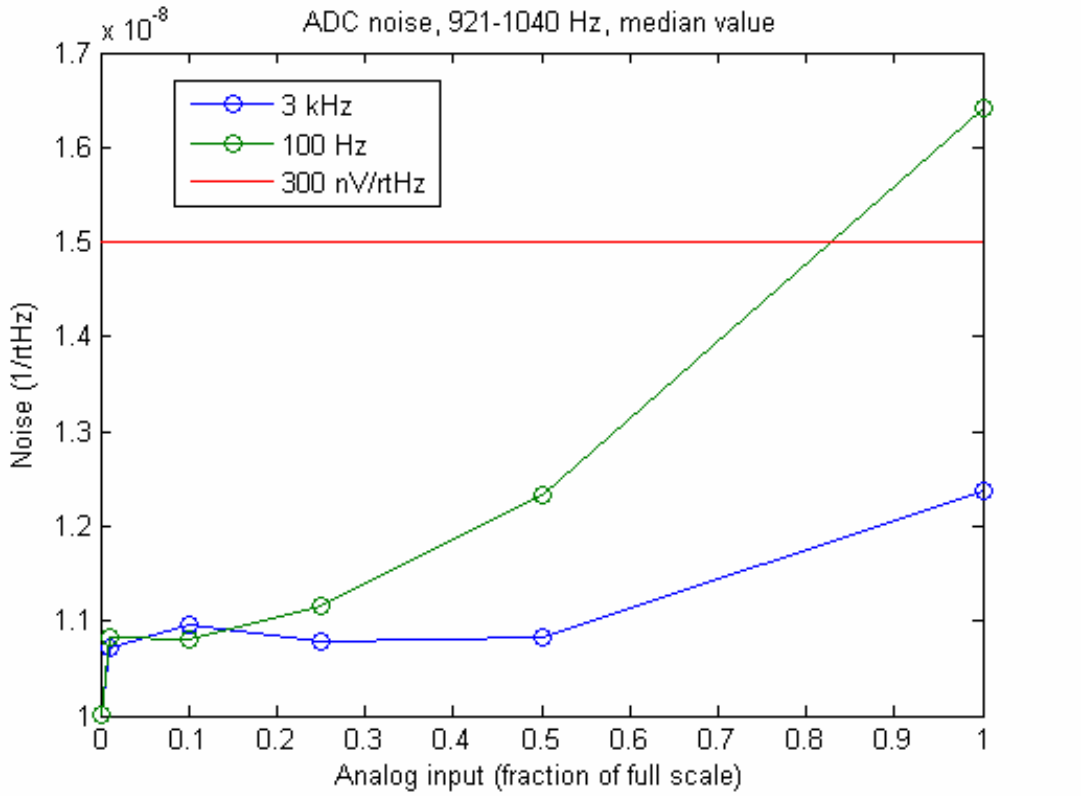

Figure 2 Plot of the analog-to-digital noise level at various input amplitudes. Data was taken from within the region of the notch. The values are measured as a fraction of full scale. The line is the goal for the noise level, equivalent to 300 nV/√Hz in a 40 V peak-to-peak range. The zero values are with no input.

the input noise at a particular frequency. The notch filter was necessary because the noise produced by the signal generator was greater than the noise expected noise from the ADCs. The filter reduces the magnitude of the noise to a level below that from the analog-to-digital converter, permitting a good measurement of the noise level in the region of the notch.

The noise level measured is within the desired range of noise levels[2], between 200 and 600 nV/√Hz in a 40 Vpp range. For lower input levels, the noise is even lower (Fig. 2). This is a significant improvement over other ADCs tested, with a noise level of 20 uV/√Hz on the same scale[5]. The specifications for the ADCs used on this test board

indicate that they should have roughly 100 dB of dynamic range for a scale of 10 Vpp[6], which is equivalent to a noise level of 250 nV//√Hz.

DAC

The digital-to-analog conversion was also examined. The analog output was tested by sending the analog signal into a spectrum analyzer. The peak was attenuated using a notch filter. This reduces the signal-to-noise ratio, matching the signal to the capability of the spectrum analyzer used. Because the notch alters the magnitude of the output, the transfer function of the notch filter must be accounted for when measuring the noise. Additionally, only regions away from the notch were considered in the noise measurement. (See Supp. Fig. 7, 9)

The resulting noise levels for a single channel are below the desired maximum noise of 600 nV/√Hz[2]. However, it is clear that more noise is present in the low-frequency region. (Fig. 3) Significant improvement may be obtained by averaging multiple channels.

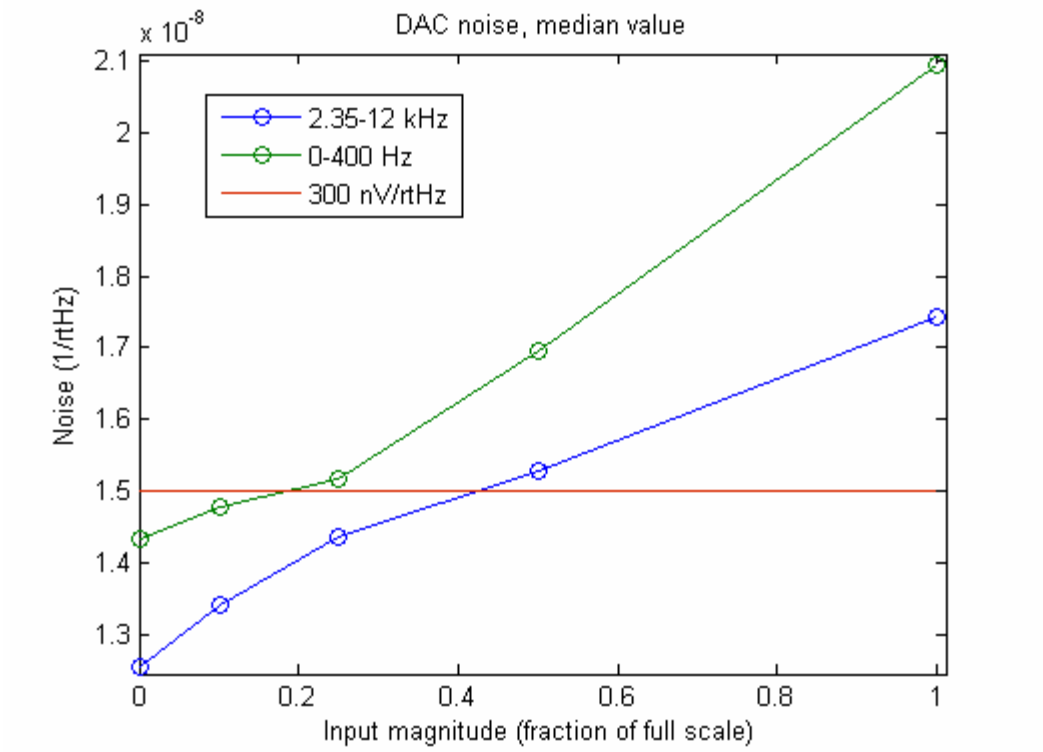

Figure 3 Plot of digital-to-analog noise levels at various amplitudes. Data was taken from stated regions away from the frequency of the notch. The values are measured as a fraction of full scale. The line is equivalent to 300 nV/√Hz in a 40 V peak-to-peak range.

Some work has already been done in averaging the signal. Adding the signals together reduces the noise level relative to the magnitude of the averaged signal. Since the converter board has four channels, they can be averaged to reduce the noise produced by the converters. If the noise from each converter is normally distributed and

independent from the noise of the other converters, the noise power will add, where power is the square of the amplitude. However, the signal, which is coherent between all four channels, will add in amplitude. As a result, when n is the number of channels averaged, the signal amplitude and the noise power both increase by n. Since the magnitude of the noise is equal to the square root of the power, the magnitude of the noise increases by √n. As a result, the signal-to-noise ratio increases by √n. Because the noise level is taken as a fraction of the full scale signal, it should be proportional to 1/√n. The averaging done for the digital-to-analog conversion performed as well as expected, decreasing the noise by roughly a factor of two when all four channels were averaged. (See Supp. Fig. 7, 8, 15)

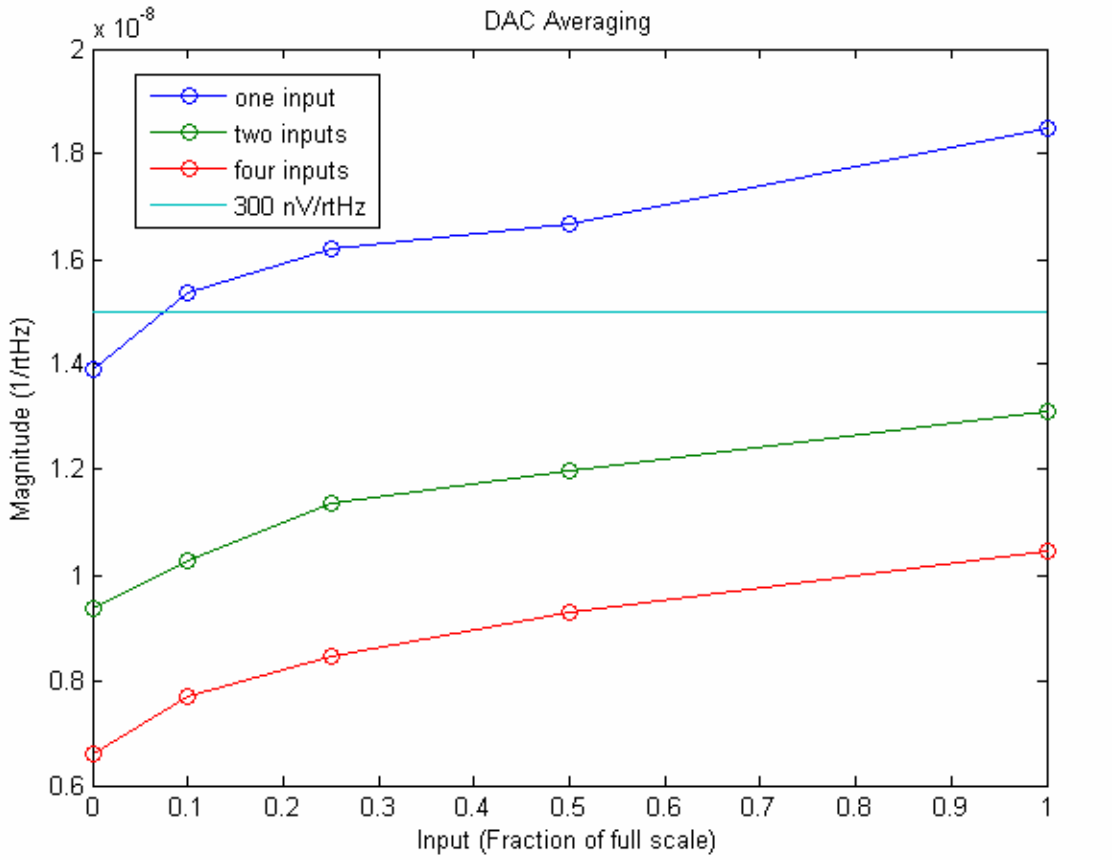

Figure 4 Digital-to-analog noise after averaging. Averaging all four channels reduces the noise level by a factor of two. Values are the median of the 2.35-12 kHz range. The line at 300nV/√Hz for 40 V peak-to-peak scale is shown for comparison.

Future work

Later work will involve more detailed testing of the converters under more varied conditions. Averaging the data from four converters, either digital-to-analog or analog-to-digital, will be examined more closely. The harmonics produced by the converters will also be analyzed. Ultimately, the data obtained will be used to produce the converter boards that will be used in Advanced LIGO.

Methods

Components Used

The analog-to-digital converter (ADC) used is an AD7679, 18-bit converter[6] from Analog Devices. The digital-to-analog converter (DAC) is a PCM1704, 24-bit converter[7] from Texas Instruments. The field programmable gate array (FPGA) is a Xilinx XC3S1500-FG320. It is on an Opal Kelly XEM3010 board[8].

FPGA

The FPGA is used with the FrontPanel software provided by Opal Kelly, the manufacturers. That software provides the tools necessary for communication with the FPGA. This includes a C++ and the components placed in the schematic. Altium Designer 6 was used to make the schematics, and, with Xilinx, produced the configuration files downloaded to the FPGA. The connection between the computer and the FPGA is a USB 2 port.

One major issue with the FPGA is that it is intended to run and control the test board using a clock running at 67 MHz, synchronized with an external one pulse per second input. In order to send and receive data from the computer, the FPGA uses first-in, first-out (FIFO) buffers to work with the timing difference between the board and the computer. When using the full sampling rate of about 524 kHz, the computer cannot communicate rapidly enough with the FPGA using the USB port, causing the input and output buffers to be emptied or overfilled. This is a serious issue for two reasons.

First, the full 4-byte value is too large to enter or leave the FIFOs as a single value, requiring it to be broken into two 2-byte words. If the words are reconstructed incorrectly, the full 4-byte value may be two 2-byte words from different original values. Any configuration used to program the FPGA for transferring data with samples greater than four bytes must take the two-word form of the data into account and using the correct byte order. When byte order and word order were incorrect, all the words were misaligned. This produced a sine wave with glitches at amplitudes where the count was an integer multiple of the number of bits in the misalignment. The problem appeared on both the ADC and DAC channels. This produced unexpected high-frequency noise until it was corrected.

Additionally, the FPGA contains a digital infinite impulse response (IIR) filter. The cutoff of the IIR filter can be seen in the ADC spectra (see Supp. Fig. 3, 5). If the input FIFO is emptied, then the IIR filter will read the last value from the buffer until new values are put into the input buffer. This produces a glitch in the DAC output. Similarly, if the output FIFO is filled, it will not read the values the filter is producing, causing a glitch in the ADC channels.

Using the FPGA's internal clock and reducing its rate until glitches are no longer observed usually prevents problems. However, synchronization with the board is desired. An alternative solution is to decimate the digital signal, so that the IIR filter deliberately reads the same value for a known number of cycles from the external clock. Decimation by a factor of four is effective in preventing errors. Decimation by eight is being used now to provide a margin for error. As a result, the FPGA is now set for a sampling rate

of 64 kHz. Since a lower sampling rate was anticipated in the final design, this is acceptable. However, code associated with the FPGA communications must continue to read the status of the FIFOs. A full or empty FIFO will be noted, in case it interferes with data transfer.

Instruments

For rough testing of the ADCs, a Stanford Research Systems DS360 low-distortion function generator was used to produce a sine wave. A Stanford Research Systems SR560 preamplifier was used to reduce some of the noise from the DS360. Later testing used an Audio Precision SYS-2722 waveform generator and spectrum analyzer, which is much cleaner than the DS360. The output of the DACs was measured using a Stanford Research Systems SR785. (See Supp. Fig. 1, 2)

Notch Filter

A notch filter with a notch at 983.083 Hz was built. It provides at least 62 dB of attenuation at that frequency. The notch filter was used on the analog side of both the DACs and the ADCs to aid in measurement. (See Supp. Fig. 11, 12, 13)

The notch filter was later modified to accept four differential inputs instead of only one. This was used to add the four DAC channels, to average the values and reduce noise. The modifications also produced a gain on each input of ¼. Full scale output would be produced by four full-scale inputs. (See Supp. Fig. 15)

ADC Testing

Testing consisted of sending a single tone input to the ADCs. Initial testing was done with a 1 kHz sine wave, and was used to confirm function and check for problems such as glitches. The ADCs themselves take input of +/- 5 V[6]. Due to gains on the board, the maximum input when using the test input was roughly 9 Vpp, and 8 Vpp was used as full scale input.

The response of the ADCs was observed at 100 Hz and 3 kHz. Input was from the SYS-2722. The performance of the ADCs was tested with full scale, half scale, quarter scale and tenth scale input, and with a 50 ohm resistor on the input to the notch filter. 18 seconds of data were sampled at a rate of 2^16 samples/second. The first 64000 samples of data were omitted from analysis to avoid errors from the initial values. This is roughly the first second of data. The following 1024000 samples, about 16 s of data, were Fourier transformed. Averaging in the power spectrum was used to reduce the number of samples above 400 (roughly 150 Hz) by a factor of 8, to reduce the number of points in the higher frequency part spectrum. The resulting samples were analyzed, approximately 128000 values. The range of values for the digital output was +/- 2^26, and normalized to +/-1 for analysis.

The noise measurement was made in a region around the notch, from 921 Hz to 1040 Hz. A median value was taken, since this is a more robust value, less strongly affected by outliers, such as harmonics, than the mean. The measurements indicated a noise level below the desired 600 nV/√Hz at a full scale of 40 Vpp. The 100 Hz signal

has noticeably more noise than the 3 kHz signal at higher amplitudes. This is most likely due to the presence of harmonics of the 100 Hz signal in the data range examined.

A copy of the schematic and appropriate configuration for the FPGA has been made which adds all four ADC channels. This averages all four signals and should reduce the amount of noise by a factor of two, as with averaging the DAC channels. It has not yet been fully tested.

DAC testing

Testing consisted of sending a digital sine wave from the computer to the board. Output was sent to the notch, then the SR785 spectrum analyzer. Full scale output prior to the notch was +/- 10 V[7]. Measurements were taken at full scale, half, one quarter, one tenth, zero amplitude and with a 50 ohm resistor across the input to the notch filter. The SR785 was set to take 800 samples. For each amplitude, measurement was made in the regions from 0-400 Hz and from 0-12.8 kHz.

The noise level of the DAC was calculated after subtracting the power of the noise from the notch filter and SR785 with the resistor on the notch's input. The noise measurement for the DACs was made in two regions, one from 2.35-12 kHz, and another from 0-400 Hz. The reason for this separation is that regions away from the frequency of the notch filter needed to be observed, since the notch significantly alters the data in that region. Additional data needed to be taken for the lower frequencies in order for the results to be significant. The median value was taken because it is more resilient than the mean to outliers from harmonics.

The noise level in the lower frequencies is significantly higher. In both regions, the noise level is below than the desired 600 nV/$\sqrt{\text{Hz}}$ [2]. This is also below the noise level for previously tested DACs[9]. When the four DAC channels were averaged, the expected twofold reduction in noise level was produced.

References

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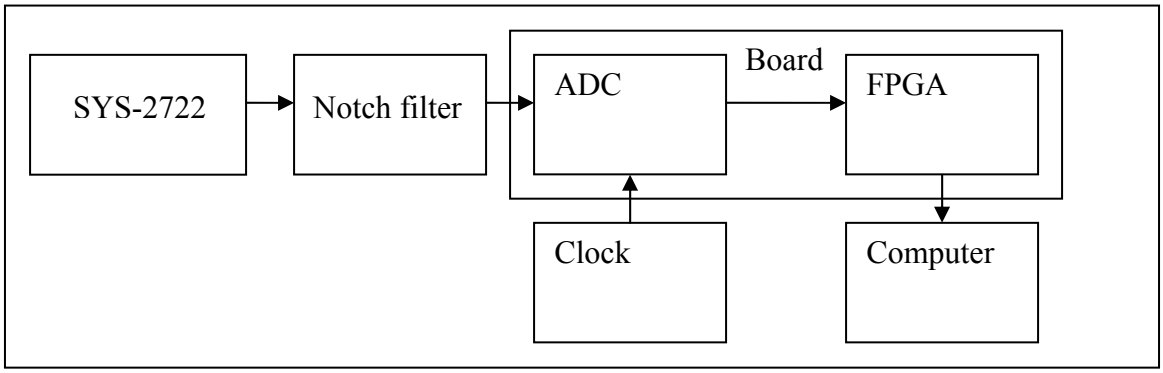
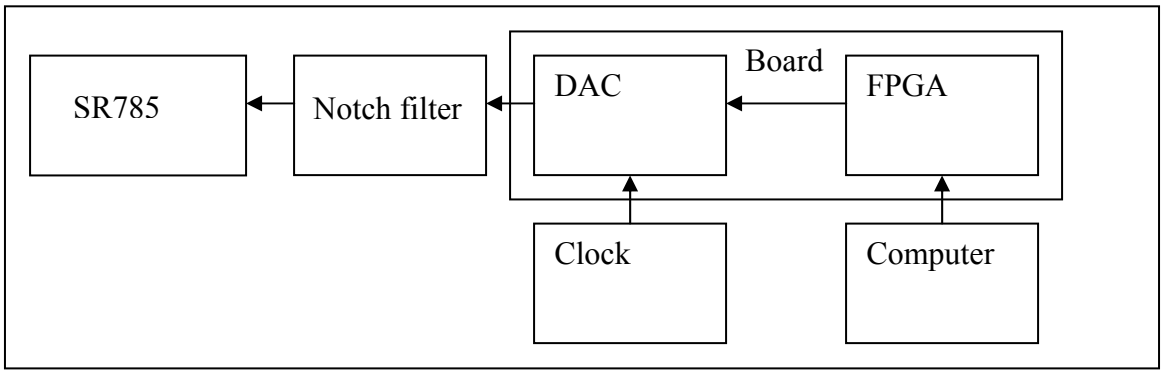
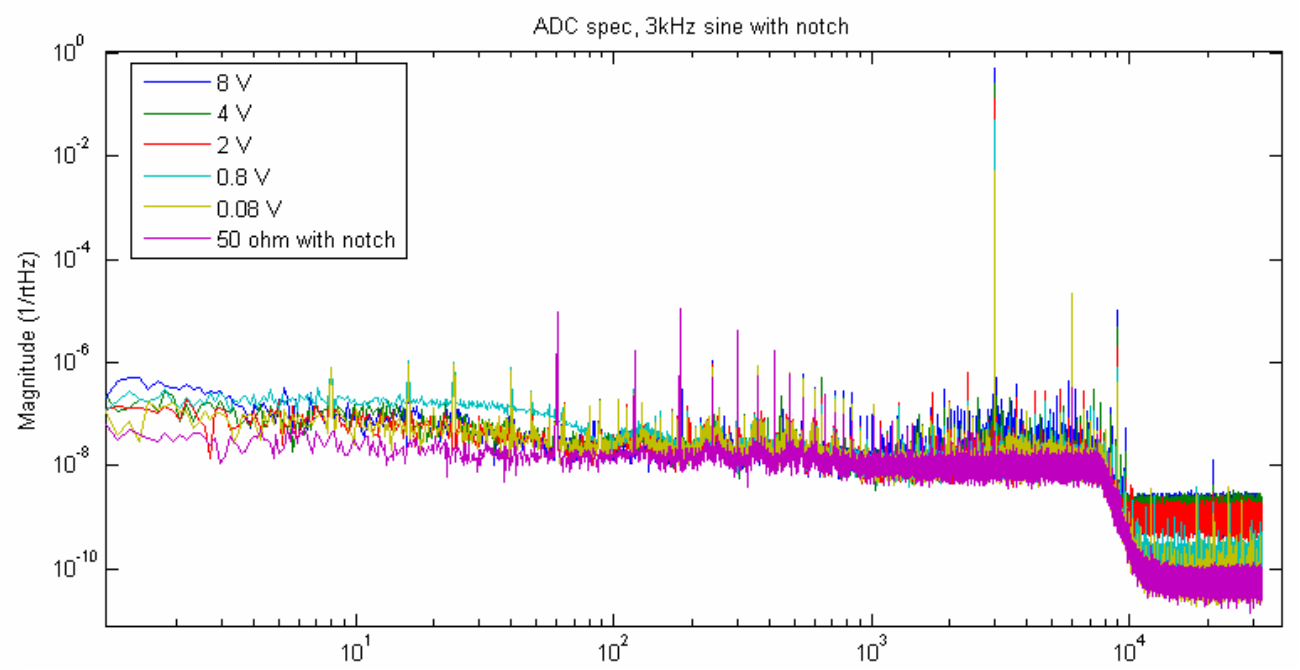
Appendix



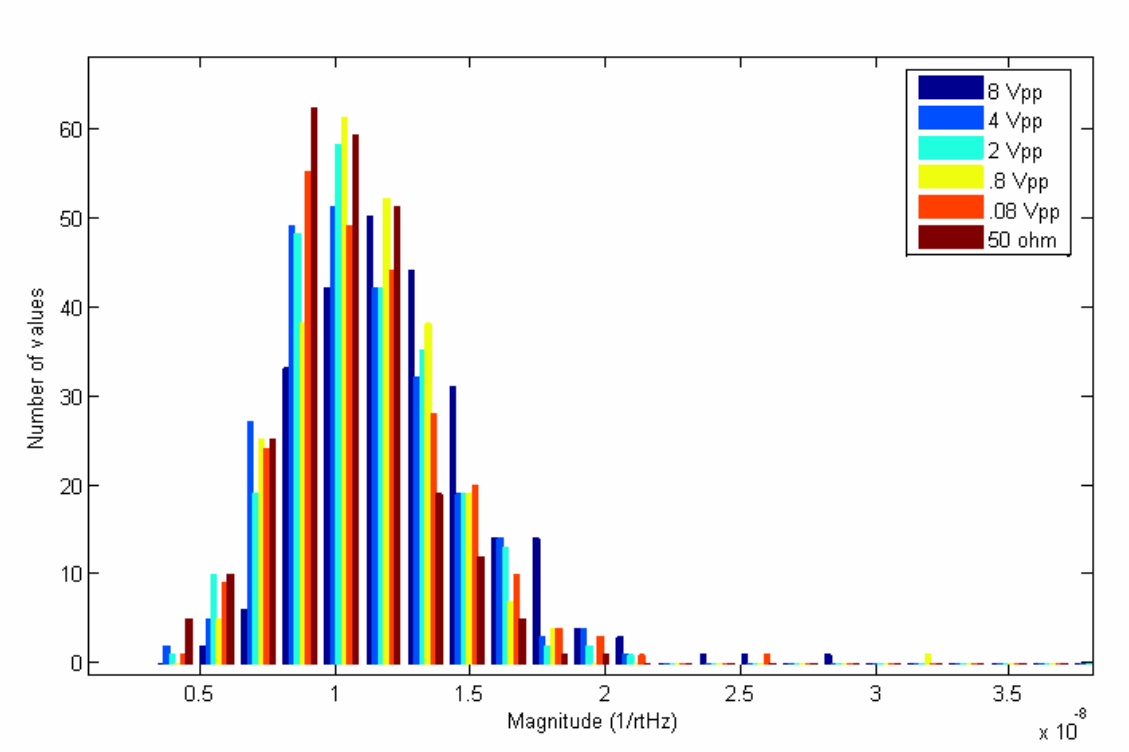
Supplementary Figure 1 Diagram of ADC testing setup.



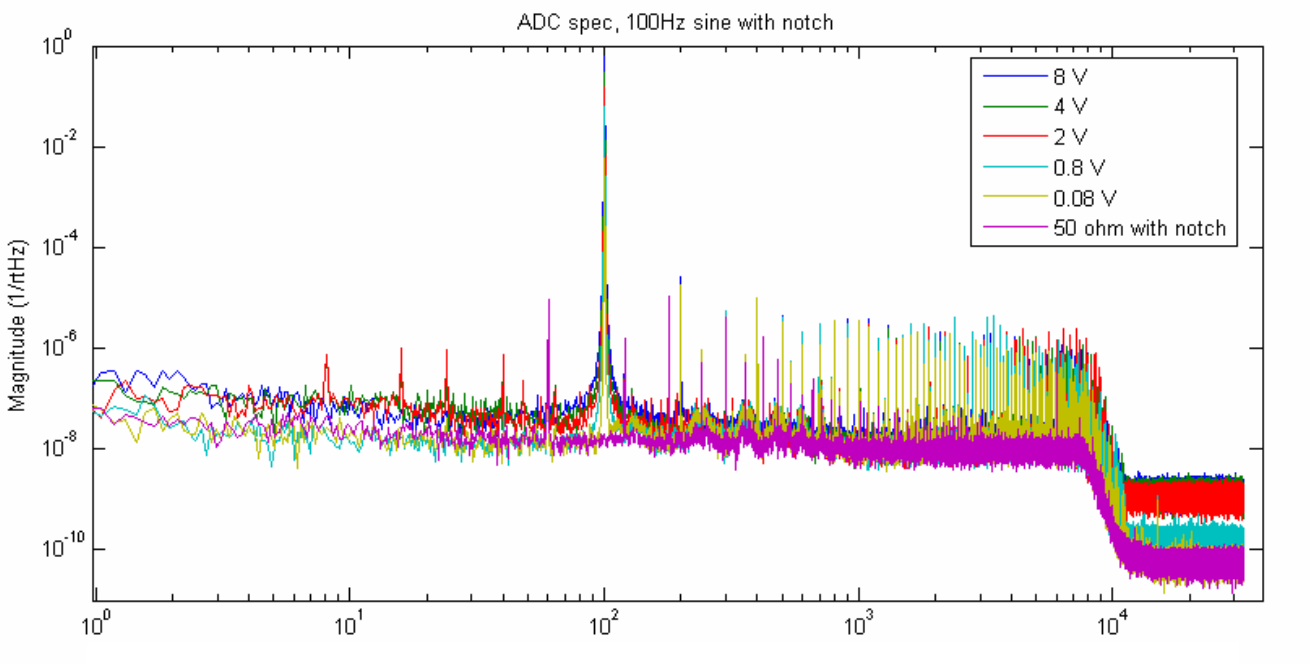
Supplementary Figure 2 Diagram of DAC testing setup.



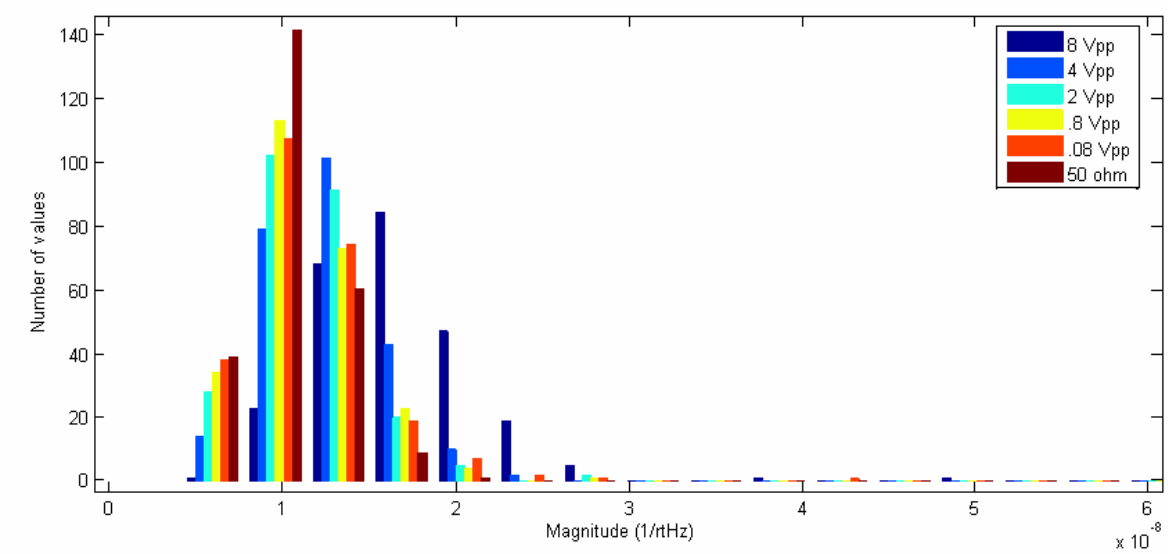
Supplementary Figure 3 Frequency spectrum of the ADC with 3 kHz input. 8 V is 8 Vpp, and taken as full scale input. The 50 ohm with notch data is the input with a resistor on the input to the notch filter.



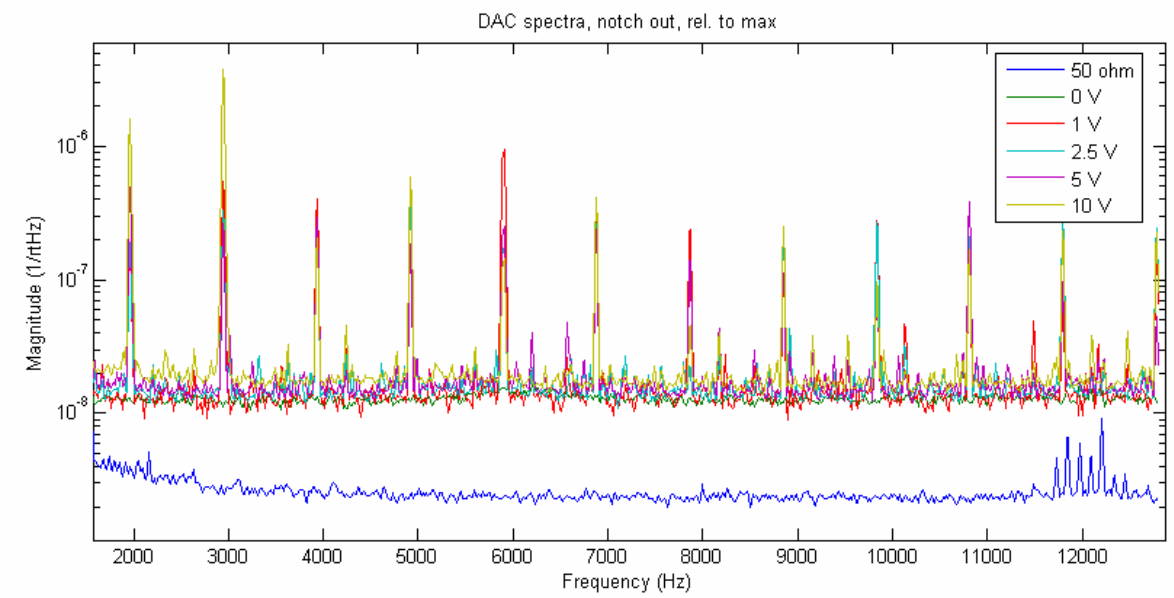
Supplementary Figure 4 Histogram of 3 kHz ADC data in the region used to determine noise level, 921-1040 Hz. There are some outlying data points not shown. Little data lies above 2.5x10^-8 1/rtHz.



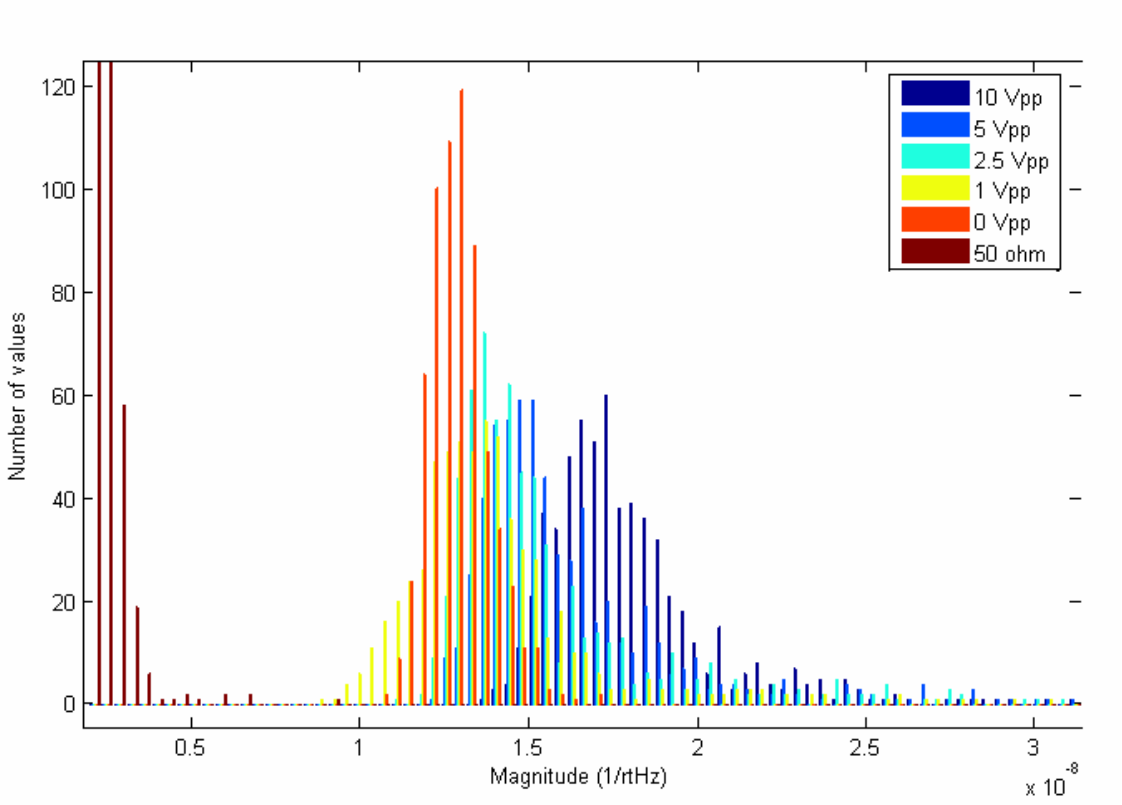
Supplementary Figure 5 Frequency spectrum of the ADC with 100 Hz input. 8 V is 8 Vpp, and taken as full scale input. The 50 ohm with notch data is the input with a resistor on the input to the notch filter.



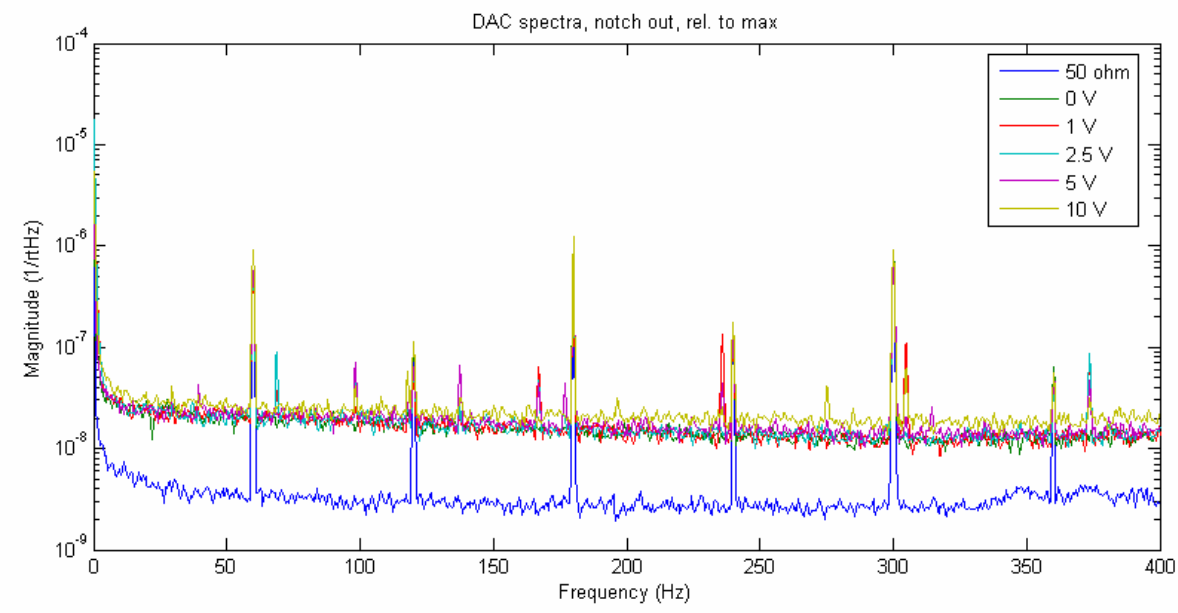
Supplementary Figure 6 Histogram of 100 Hz ADC data in the region used to determine noise level, 921-1040 Hz. There are some outlying data points not shown. Little data lies above 3x10^-8 1/rtHz.



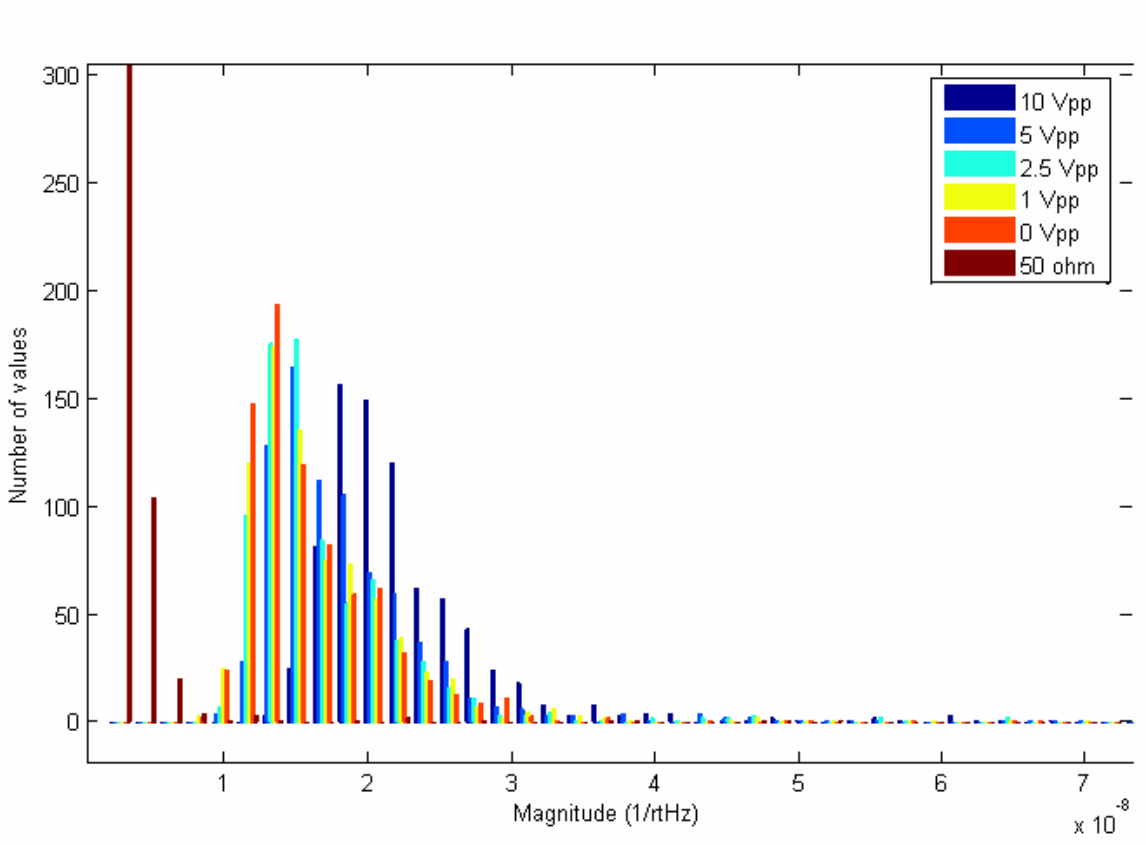
Supplementary Figure 7 DAC spectrum above 2 kHz. The transfer function of the notch has been accounted for in this plot. Input is in Vpp. The 0 V spectrum is with the amplitude of the digital sine wave set to zero. The 50 ohm data is from placing a resistor on the input to the notch filter. The digital sine was set to the notch filter's deepest frequency, 983.083 Hz.



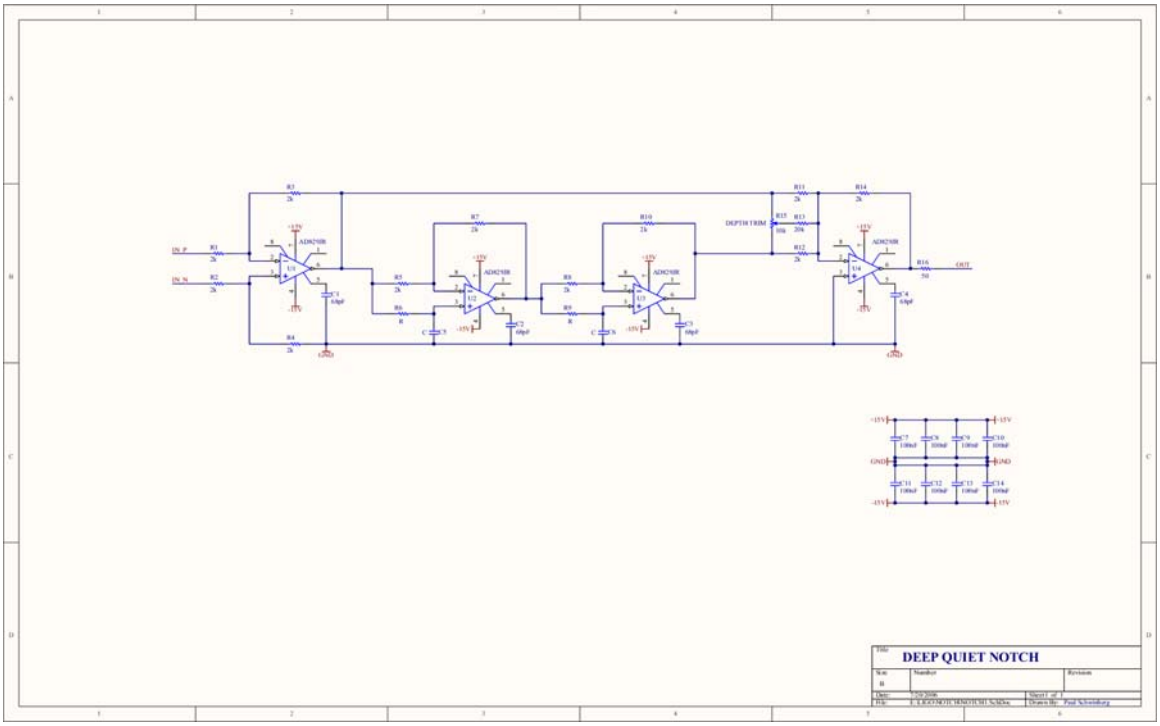
Supplementary Figure 8 Histogram of DAC data above 2.3 kHz used in determining the noise level. The two lower bars for the 50 ohm data set reach roughly 200 and 350 values. 650 values total were used.



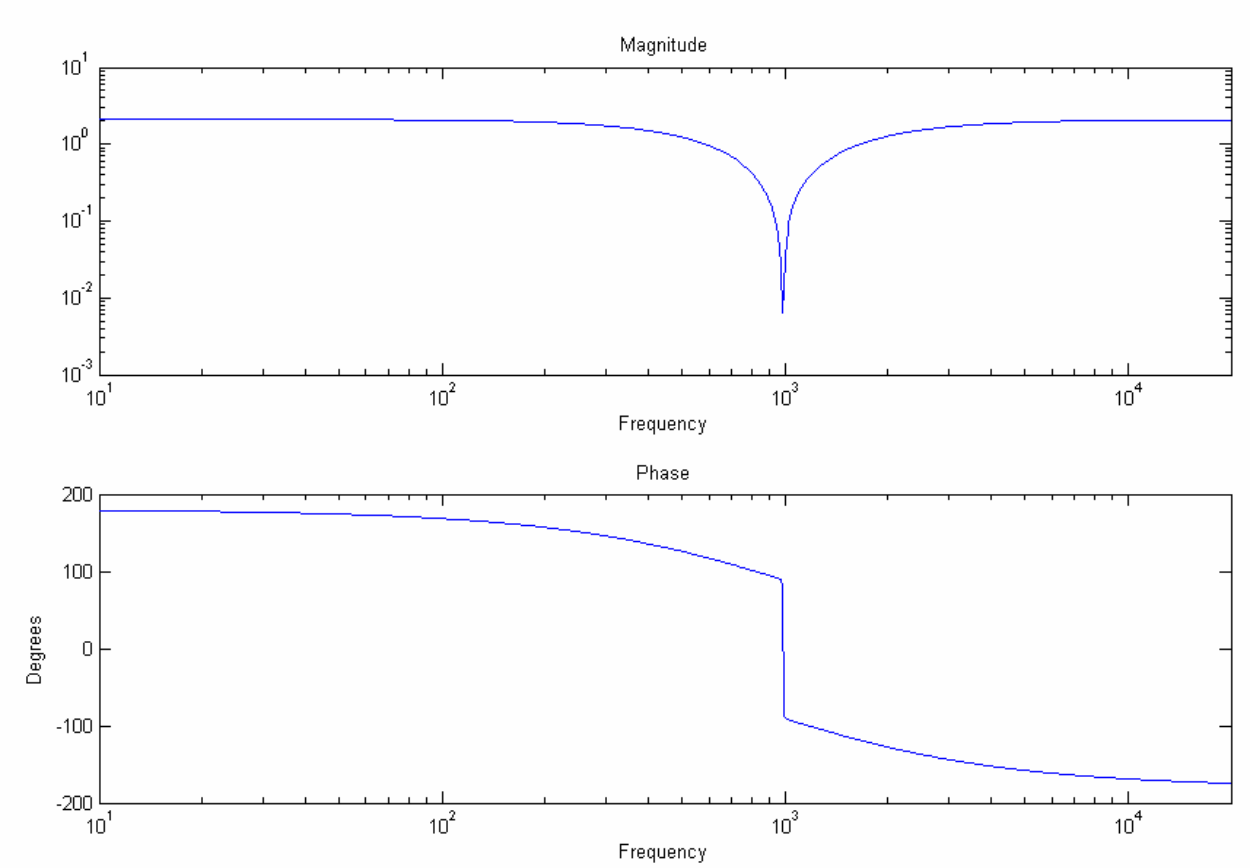
Supplementary Figure 9 DAC spectrum from 0-400 Hz. The transfer function of the notch has been accounted for in this plot. Input is in Vpp. The 0 V spectrum is with the amplitude of the digital sine wave set to zero. The 50 ohm data is from placing a resistor on the input to the notch filter. The digital sine was set to the notch filter's deepest frequency, 983.083 Hz.



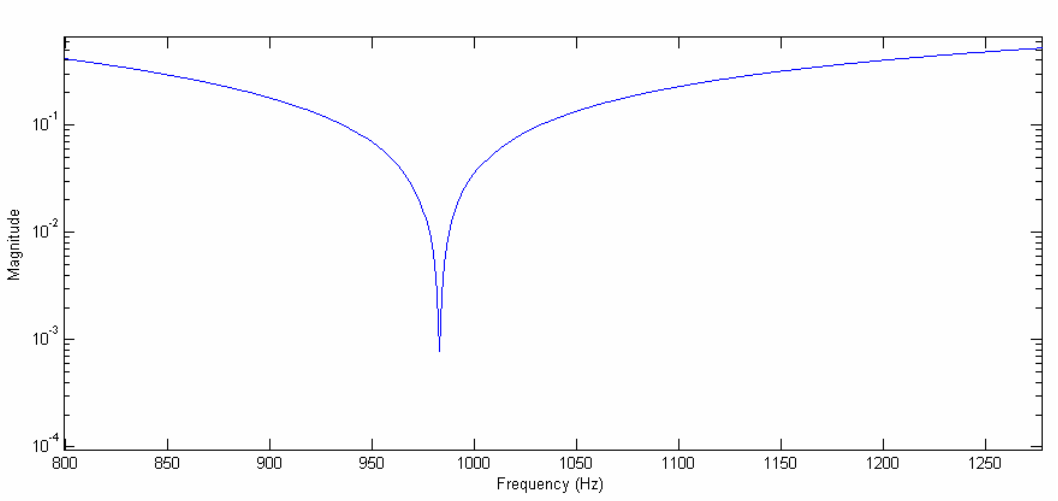
Supplementary Figure 10 Histogram of DAC data from 0-400 Hz used in determining the noise level. The lowest bar for the 50 ohm data set includes roughly 650 values. 800 values total were used.



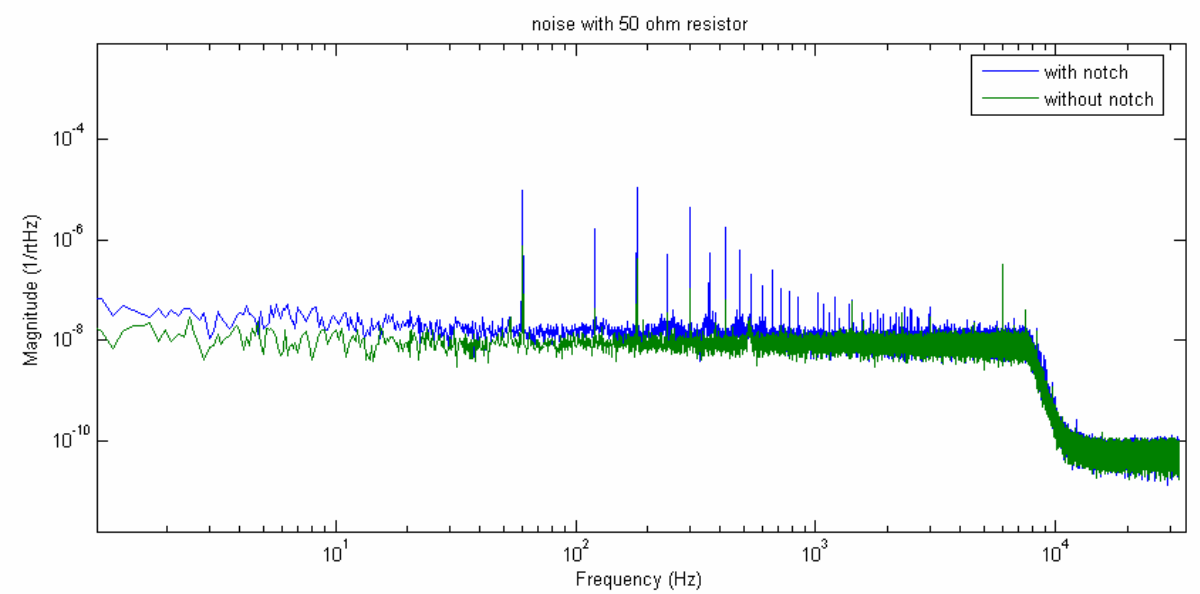
Supplementary Figure 11 Schematic of the notch filter.



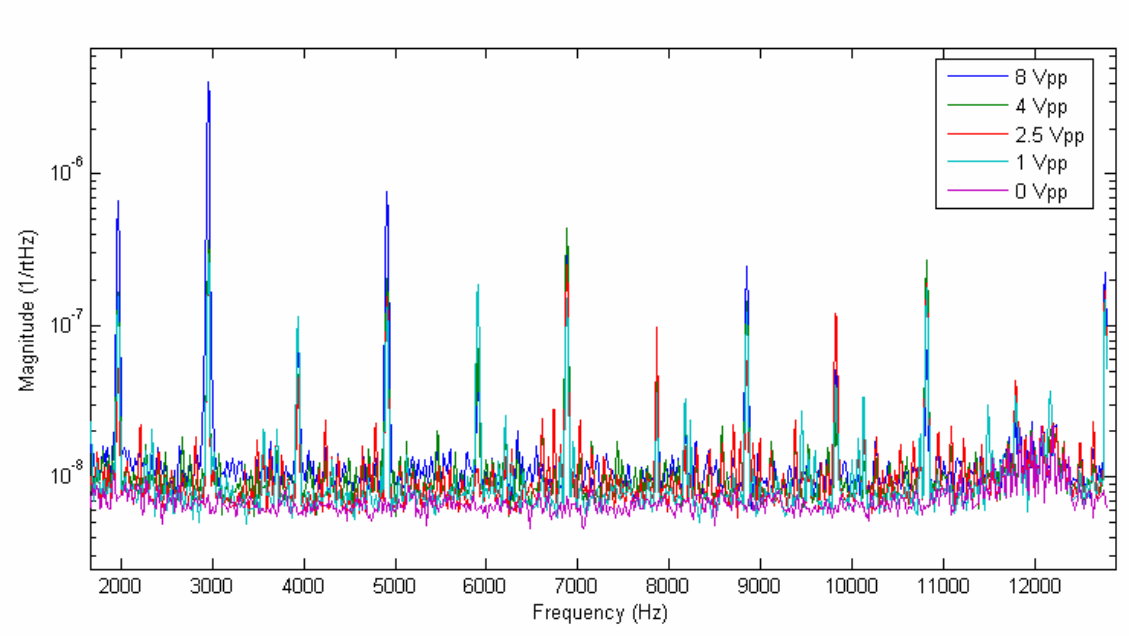
Supplementary Figure 12 Transfer function of the notch, measured using the SR785.



Supplementary Figure 13 Closer view of the transfer function of the notch, around 983 Hz.



Supplementary Figure 14 Comparison of noise with and without the notch filter.



Supplementary Figure 15 Averaged spectrum for the DACs. This plot shows the result of averaging all four DAC outputs.