LASER INTERFEROMETER GRAVITATIONAL WAVE OBSERVATORY
- LIGO -
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ISC - DAQ Interface

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ISC / CDS

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1 INTRODUCTION

Since most of the interferometer controls will be implemented digitally, it makes sense to integrate the need for a digitizer of both the ISC (interferometer sensing and control) and the DAQ (data acquisition) subsystems in one common front-end. This document presents a conceptual design for such a system and works out the advantages and disadvantages this approach has over two independent implementations.

By integrating the front-end of two subsystems one has to look at the following issues:

1) Global networking: defines the points of interaction and the global data flow.
2) Actual interface implementation: addresses the sharing of hardware/software at the front ends.
3) Synchronization: defines the dynamic behavior/interactions of the two systems.

Due to the real-time nature of the ISC system and the fact that the servo system has to handle signals at their full dynamic range, the ISC system puts higher demands on the digitization process than the DAQ system. Naturally, it is then the ISC system which is responsible to perform the actual digitization. The DAQ system will only periodically read the sampled data provided by the ISC system through, e.g., a reflected memory module.

This approach has the following advantages:

- Avoids duplicated digitization efforts, i.e. reduces number of electronics components.
- No problems with data consistency, i.e. clear data interface.
- Diagnostics subsystem can fully rely on DAQ system for (low bandwidth) data taking.
- Adds flexibility through (possible) data processing in the front-end.
- DAQ system independent of ISC implementation details.
- DAQ system takes full advantage of ISC capabilities.
- ISC system doesn't have to provide special analog signals which are sampled again by the DAQ system.

And the following disadvantages:

- Timing control (GPS clock) has to be implemented in the ISC front-end.
- Higher level of integration between ISC and DAQ necessary.

We feel that the advantages predominate. In the following sections a conceptual design of an ISC-DAQ interface is worked out in more detail.

2 NETWORKING AND DATA FLOW

A schematic view of the data flow is shown in Fig. 1. The ISC data read by the DAQ system originates either directly at the front-end (sensor signals), at the back-end (suspension control signals) or at the servo compensation (servo status signals). Since sensor and controller signals are measured and applied at different physical locations, but are all routed through the servo controller, the DAQ system could conveniently interfaces the ISC system at the LSC and ASC servo controller only (see Fig. 2). This might require that additional information (such as the signals of the shadow sensors) has to be transferred back from the suspensions to the servo controller. This might not be a real drawback, since this information might be needed by the ISC system anyway. Of course, bandwidth limitations might still require a parallel network for the

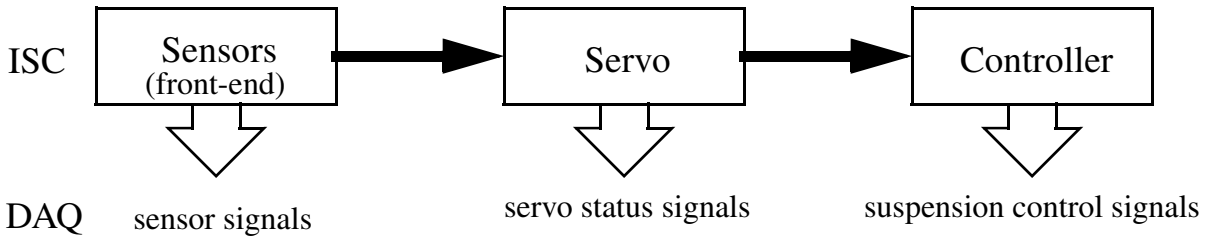

Figure 1: Global flow of information common to ISC and DAQ.

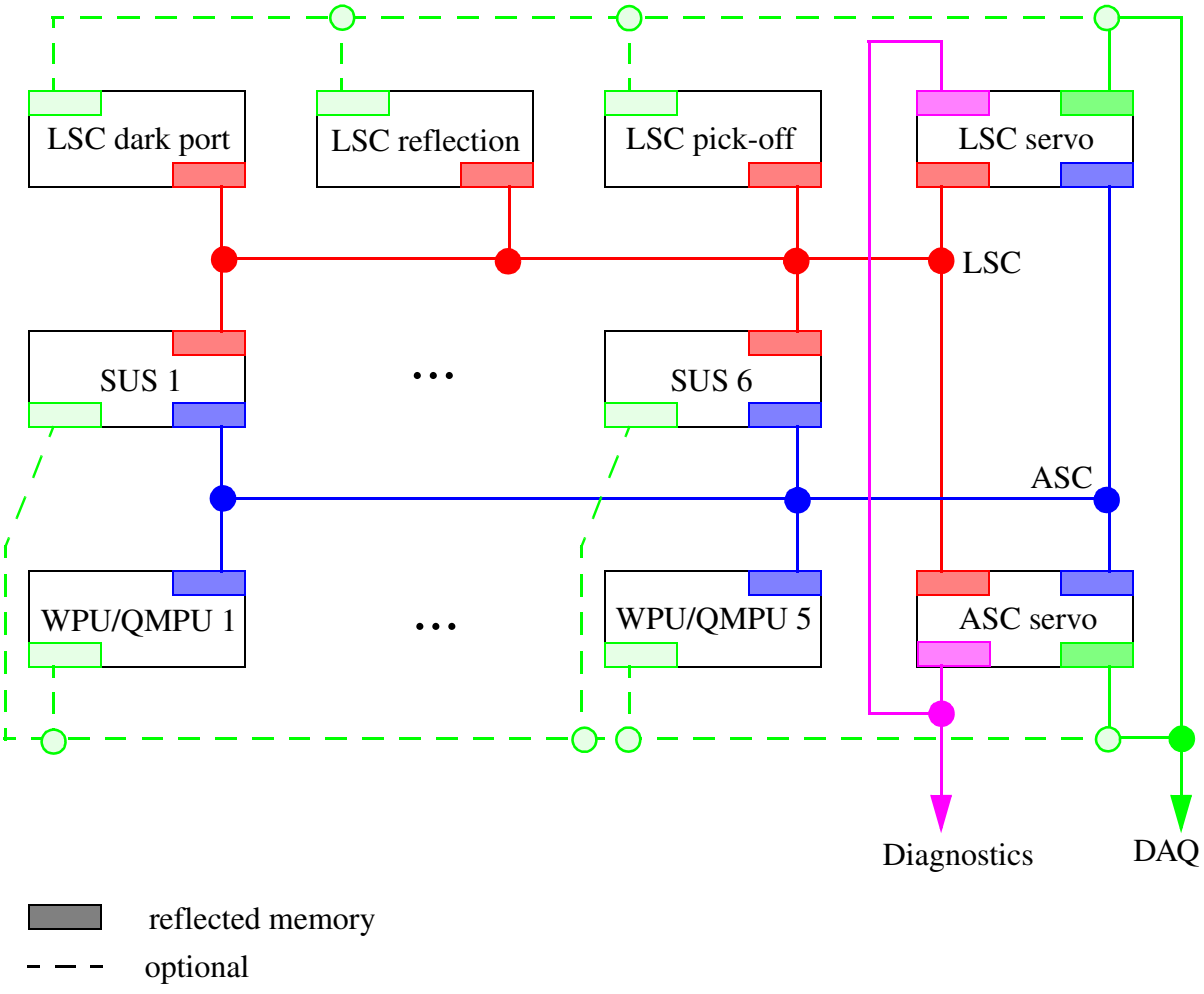

Figure 2: Networking and interfacing for LSC, ASC, DAQ and diagnostics.

DAQ system. Fig. 2 also shows two independent networks for the LSC and the ASC subsystems. However, both networks are connected to both servo controllers, so that each system is able to see the other at a high bandwidth which might come handy when implementing a guided lock acquisition algorithm. Optionally, if bandwidth is sufficient, both networks could be integrated into one. The diagnostics system interfaces the ISC system at both servo controllers. This should allow enough bandwidth for the diagnostics system to read any ISC sensor or control signal. Additionally, stimulus of LSC and ASC servo loops can be generated directly in the servo controller and read back through the diagnostic system.

3 INTERFACES

3.1 DIGITIZATION OF ISC SIGNALS

Due to the high power at the dark port its length photodetector will consist of an arrangement of multiple photodiodes. In Principle, one could add the analog readout channels before they are sampled by the ADC. However, sampling each channel individually and then add the signals digitally has several advantages: First, the digitization noise is suppressed and, second, diagnostics of the photodiodes is greatly simplified. Furthermore, fine-tuning of gain and rf-phase differences can be easily done in software. A sketch of the dark port length detector is shown in Fig. 3; in this case 8 individual photodiodes and 16 readout channels (in- and quad-phase have separate channels) are laid out. The 16 bit ADCs work close to the highest possible sampling rate to minimize the quantization noise. Since this rate is higher than the required rate for both LSC and DAQ, the data are decimated after a digital filter stage. Finally, the quad-phase signals are added to form the dark port error signal and are transferred to the LSC servo controller and the DAQ system.

The length sensors in reflection and at the power recycling cavity will have a similar layout. For the ASC system the wavefront processing units (WPU) and the quadrant and monitor processing units (QMPU) will serve as the digital front-end utilizing the same or similar techniques. This approach greatly simplifies the implementation of the DAQ system, since for most of the high bandwidth ISC channels the data will be available in digital form. The preferred networking solution of both ISC and DAQ is a reflected memory system. Therefore, it should only be a small increase in complexity to add additional reflected memory modules belonging to the DAQ system into the servo controllers (or optionally also the front-ends) of LSC and ASC. In case, the interface points are located at the front-end, the ISC front-end processors will write the measured data to the reflected memory modules of both ISC and DAQ. In case, the interface points are solely located at the servo controllers, the servo controller copies the data from its reflected memory module into the one of the DAQ. This should not pose special timing problems, because the DAQ frame builder reads its data in 1 second intervals (buffers) only.

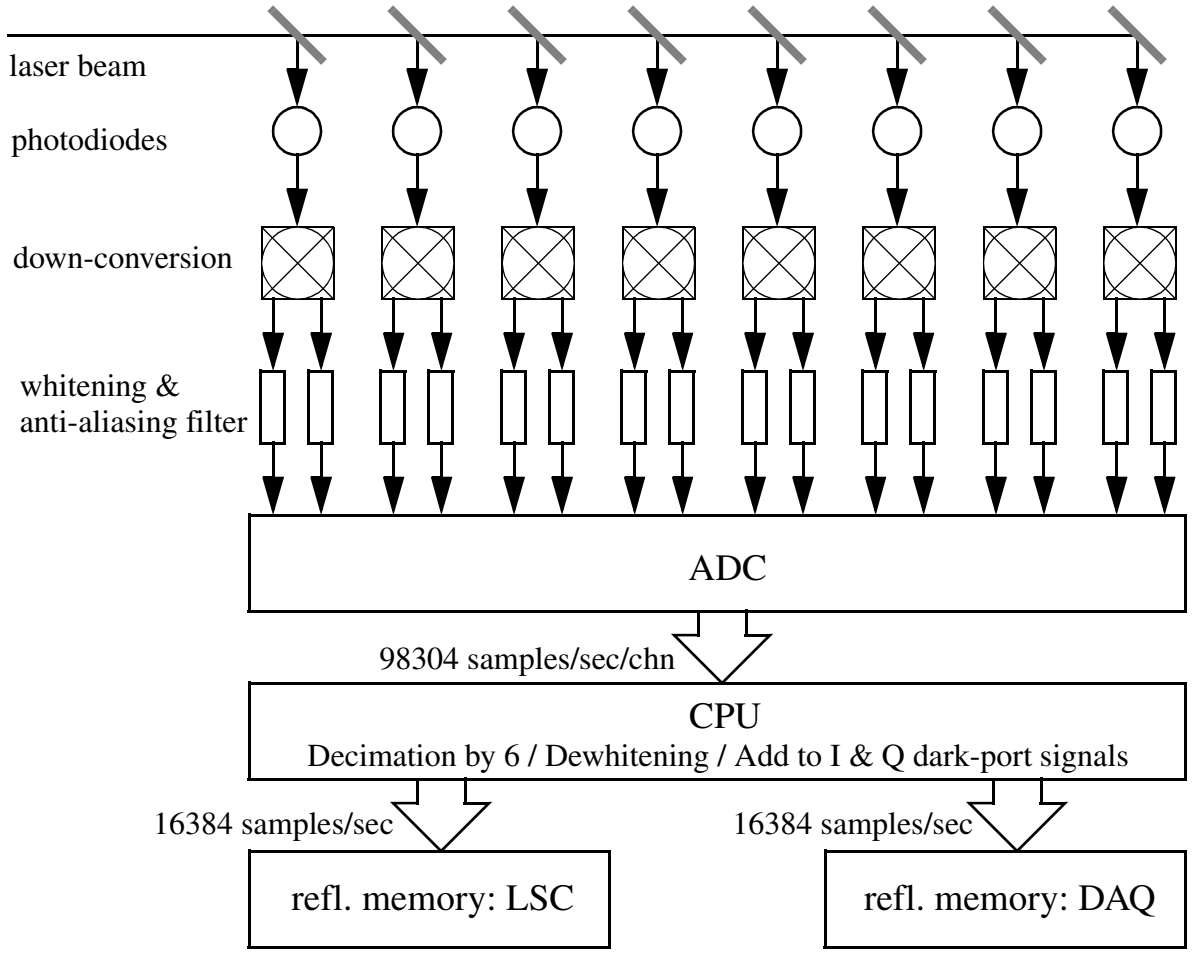

Figure 3: Sketch of the dark port length detector.

3.2 Unified Digital Interface to the Suspension Controller

Presently, the suspension controllers are implemented in analog. Consequently, since both LSC and ASC are implemented in digital form, ISC has to provide digital-to-analog converters to interface the suspension controllers. This makes this system vulnerable during future upgrades of the suspensions to, say, a double pendulum. Furthermore, future suspension controllers will most likely use digital technology themselves. A better approach then seems to unify the suspension interface into one single digital controller. A sketch of such a digital suspension interface (DSI) — based on the present analog implementation — is shown in Fig. 4. A VME based CPU is responsible to read the control signals from reflected memory modules belonging to the LSC and the ASC systems and to write them into the angle and length DACs. To further simplify the interface the local suspension sensors (shadow sensors) are read back by the same DSI and written in to the corresponding reflected memory modules. Adding the readout and control of the optical

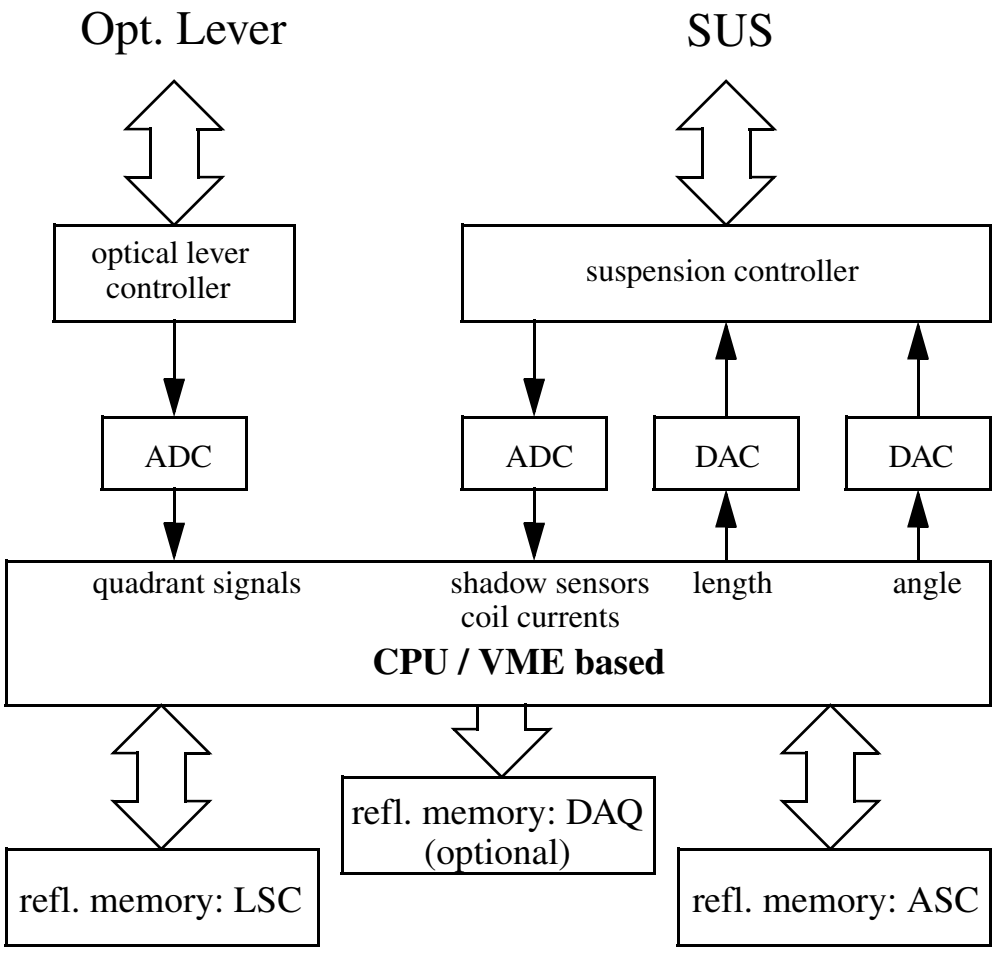

Figure 4: Unified digital interface to the suspension controller (DSI).

levers to the DSI makes the suspension controller a stand-alone unit which will make it possible to perform simple alignment and calibration tasks (through EPICS control) without relying on the presence of the rest of the ISC system. This feature seems especially important during initial setup of the suspensions when it is unlikely that the full ISC system is already in operation.

4 TIMING AND SYNCHRONIZATION

The timing requirements of a servo system is of course completely different from the one of data acquisition system. In the former case data have to be transferred in real-time to avoid delays in the feedback path and, therefore, possible oscillations in the loops. In the later case the data can be stored in a local buffer and periodically be transferred as a whole block when a certain time — in our case 1000 ms — has passed (see the timing chart in Fig. 5). Since in the design presented here the ISC system is responsible for the data sampling, the data preprocessing and the data transfer into the reflected memory common to ISC and DAQ, the full data of a block might not be ready

immediately after the last sample of the block. An additional latency has to be incorporated into the design, before the frame builder of the DAQ system is allowed to begin reading the data from the reflected memory. A latency of about 500 ms seems adequate, allowing enough time for the ISC system to prepare the data and at the same time avoiding an excessive delay in the DAQ system. During this latency the frame builder doesn't necessarily have to stand still; indeed, it can first fetch the data provided by analog subsystems which are interfaced directly by the DAQ ADCs.

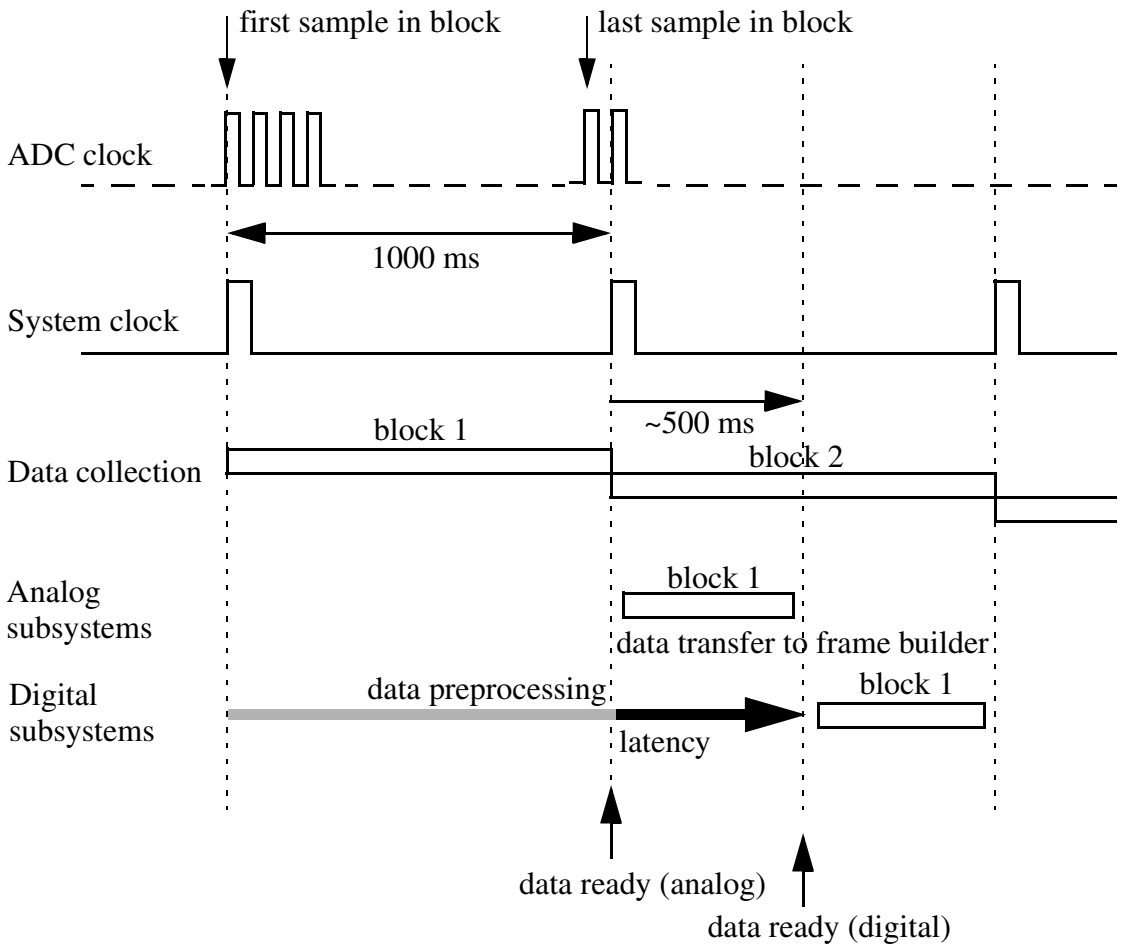

Figure 5: Global DAQ timing chart for data collection and transfer.