
Fiber Based Synchronous Timing System

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- Timing jitter from ISC fanout (2 pin LEMO fanout) and Variable Delay Timing Module < 50ps
- GPS Clock Driver board similar in complexity to previous two boards, expect similar results
- Absolute error in GPS clock is $\pm 155 \text{ ns}^1$
- Overall performance isn't that bad

1) T010034-00D, Timing system test at the second engineering run (E2) at LHO

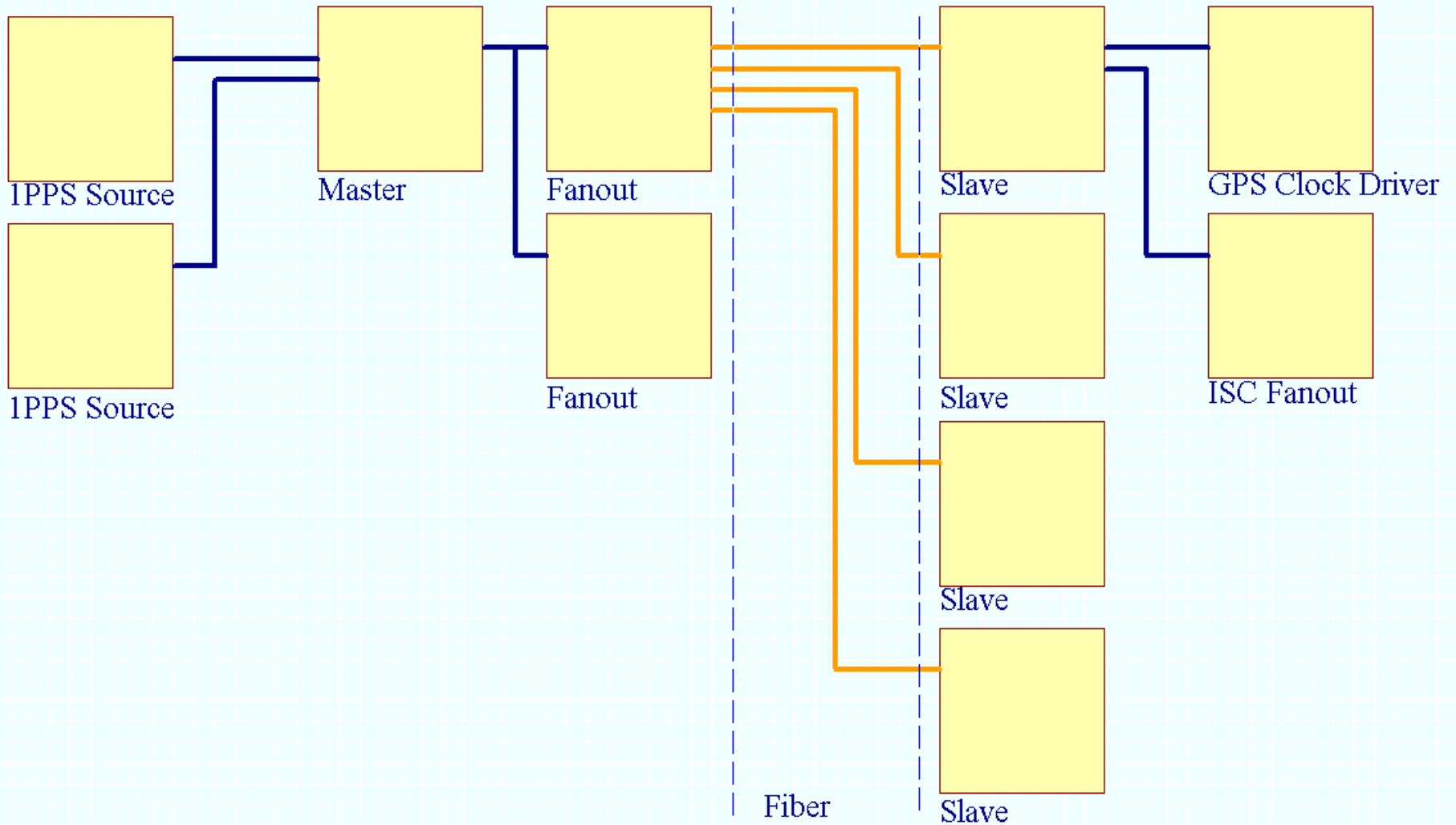
- Some problems with existing system
 - » Timing glitches cause channel hopping, etc.
 - » Locked into using Brandywine GPS receiver
 - » Lack of realtime diagnostics to monitor status
 - » No active diagnostics comparing building synchronization

- Should be at least as good as current system
 - » Absolute error $< \pm 155$ ns
 - » Additional jitter < 50 ps
- Goals from Daniel's proposal
 - » Provide a time stamp aligned with UTC to within better than 1us
 - » Provide a means to synchronize the front-end ADCs and DACs in hardware
 - » Provide a reliable link to distribute the timing signal from a single source
 - » Provide the capability to use commercial GPS units or an atomic clock as the timing standard
 - » Provide diagnostics to monitor the status of the timing system
- Not enough time to implement it all before S5

Major Goals of this System

- Maintain accuracy of the current system
 - » Improve synchronization between corner station and outbuildings
- Provide a reliable link to distribute the timing signal
 - » Eliminate potential ground loop problems
- Capability to use any 1PPS signal as source
 - » Frees us from the Brandywine GPS receiver
- More diagnostics

Block Diagram



Task List	4/4 – 4/8	4/11 – 4/15	4/18 – 4/22	4/25 – 4/29	5/2 – 5/6	5/9 – 5/13	5/16-5/20
Present Conceptual Design and System Requirements							
Design Master/Fanout/Slave (Schematics and Layout)							
Send Out Preliminary Schematics/Layout							
Present Preliminary Design and Finalize System Requirements							
Send Out Prototype Schematics/Layout							
Prototype Final Design Review							
	5/23 – 5/27	5/30 – 6/3	6/6 – 6/10	6/13 – 6/17	6/20 – 6/24	6/27 – 7/1	7/4 – 7/8
Design Master/Fanout/Slave (Schematics and Layout)							
Software Development							
Manufacture Master/Fanout/Slave Prototype							
Write Test Plan for Prototype System							
Test Fiber Based Timing System Prototype							
Results and Final Design Review							
	7/11 – 7/15	7/18 – 7/22	7/25 – 7/29	8/1 – 8/5	8/8 – 8/12	8/15 – 8/19	8/22-8/26
Software Development							
Manufacture Master/Fanout/Slave							
Write Test Plan for Final System							
Test Fiber Based Timing System							
Installation and Finalize Documentation							

	Single Mode System	SM & MM Based System
Master Prototype	\$1,671.00	\$1,671.00
Fanout Prototype	\$3,775.00	\$3,135.00
Slave Prototype	\$2,071.00	\$1,911.00
Master	\$4,157.00	\$4,157.00
Fanout	\$24,375.00	\$21,634.00
Slave	\$27,210.00	\$22,410.00
Grand Total	\$63,259.00	\$54,918.00

- SM fiberoptic transceivers account for 44.3% of the total cost of the SM system (~\$28,000.00)
- Same SM transceivers account for 25.1% of mixed system budget (~\$13,800.00), still a significant portion
- Transceivers are interchangeable, can easily convert SM to MM and back
- Does not include ~\$2000 for fiber

- Decide on final form factor
 - » VME for all cards?
 - Dedicated crate in aux rack
 - Never needs to be powered down
 - Possibly EMI interference with master
 - Will have EMI shield
 - » Master in dedicated 1U chassis
 - Needs own supply
 - Complicates the interface, can't use VME backplane
 - Uses up more vertical rack space in addition to needed VME crate
- SM vs. SM/MM implementation

- What diagnostics to add?
 - » Slaves will have signal detect and 1PPS
 - » Should probably have synch detect
 - » Will report errors in 1PPS

- Slave board nearly complete
 - » Needs VME interface
 - What address and data sizes to use?
 - Copy existing system of A16/D32 on other boards?