

LAPP R&D – Virgo+ Online architecture

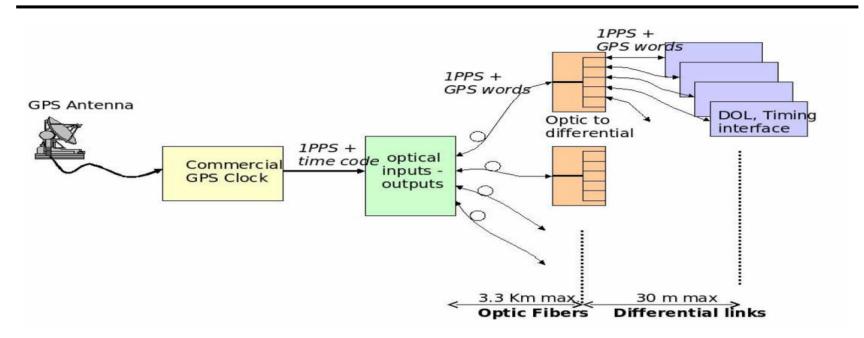
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LIGO-G070345-00-Z



LAPP R&D – Hardware status

New Control and DAQ electronics – Timing system



- 2 signals distributed overall the ITF:
 - 1PPS(IRIG-B) for the local clock synchronization and the absolute time stamp
 - A fast clock (10MHz) as centralize fast clock synchronized on the GPS
- Optical fibers and differential cables distribution
- Linear power supply

(0)



- Signal generator SW1050-R-10 from MicroSystems
 - GPS Motorola M12T receiver
 - Rubidium clock



- Fully tested:
 - IRIGB frame updated with the GPS and ULeaps fields
 - No more time stamp errors
 - 1 or 2 jumps of 130ns per week on the 1PPS position in the IRIGB frame
- 2 others signal generator to purchase: 7-8KEuros per generator



- Distribute the timing signals between the buildings and inside a building
- Prototype fully tested:
 - minor modifications on the PCB



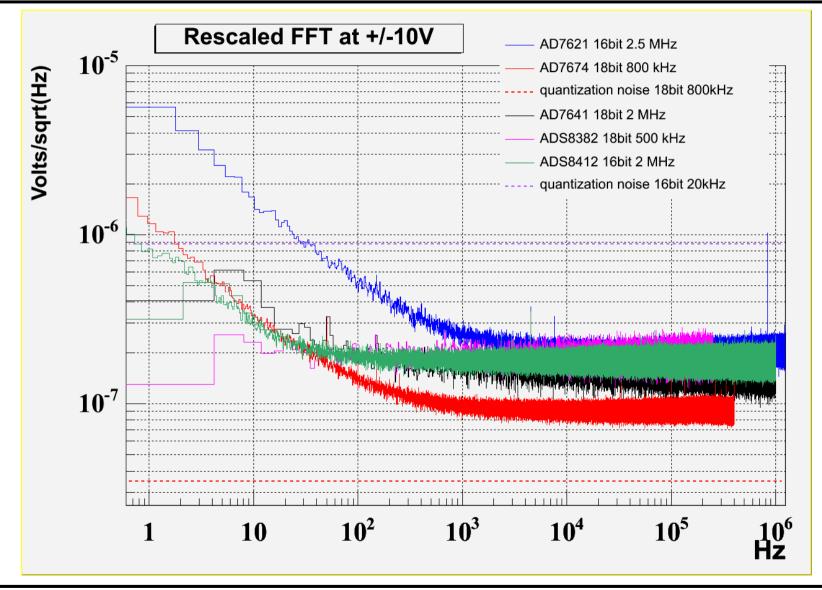
- Performances:
 - Phase jitter between 2 TDBs over 1m of RJ-45 cable: 18,4ps
 - phase jitter between 2 TDBs over 3Km of fiber : 58.4ps
- First estimation: 11 TBD A @0.8KEuros 11 TDB B @1.2KEuros:42.8KEuros



- Higher sampling frequency with embedded shaping/emphasis facilities
- ADC selection done: AD7674 18bit @ 800kHz
- 16 differentials channels with analog anti-alias filter at 400KHz
- Differential or single-ended input
- Digital anti-alias filters in embedded DSPs(4 channels per DSP ADPS-21262 @150MHz)
- On board Timing system to stamp data with the GPS time
- Communication through optic fiber for data transmission and board configuration
- First estimation: 68 ADC @1.8KEuros : 122.4 KEuros

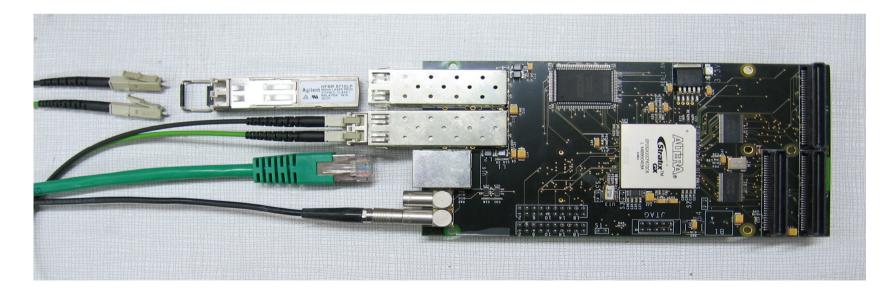


ADC board – ADC selection





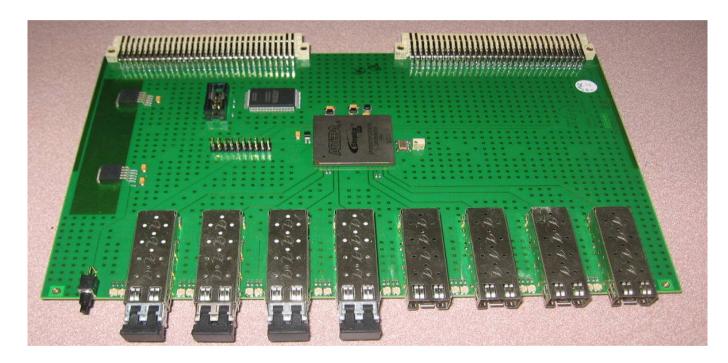
- Prototypes currently used for ADC tests, TOLM /DSP interface tested
- Upgrade with 1.6Gbit/s on the optical link and PCI 64bits@66MHz
- 2 types of TOLM: one as PMC format(v1), one as PC-PCI format(v2)
- TOLM Timing jitter: 15ps at the TOLM output 30ns between two TOLMs with locked oscillator



First estimation: 41 TOLM-v1 @0.9KEuros – 35 TOLM-v2 @0.9KEuros: 68KEuros



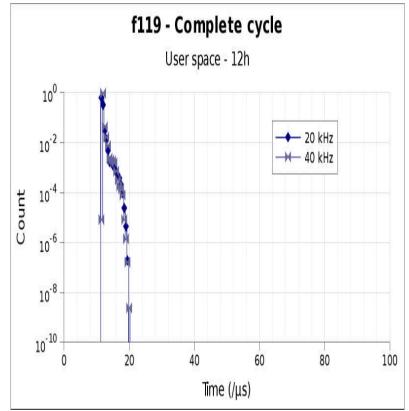
- Improve the data access path: optical links router between TOLM interface
- Electronic tests ok



- Full prototype tests: mid-June 07
- First estimation: 32 MUX-DEMUZ @1.6KEuros :51.2KEuros



- Transtec: dual core opteron @2GHz
- Kernel tunings: RTAI "vanilla" Linux kernel Scientific Linux 4
- CPU allocation:
 - On core involved for real-time operation with the real-time interrupts routed to this CPU only
 - One core for DAQ and Linux without real-time interrupts routed on it
- Test the full Pr and Gc configurations up to 40KHz : maximum expected time: 22us with 14MBytes/s of compressed data

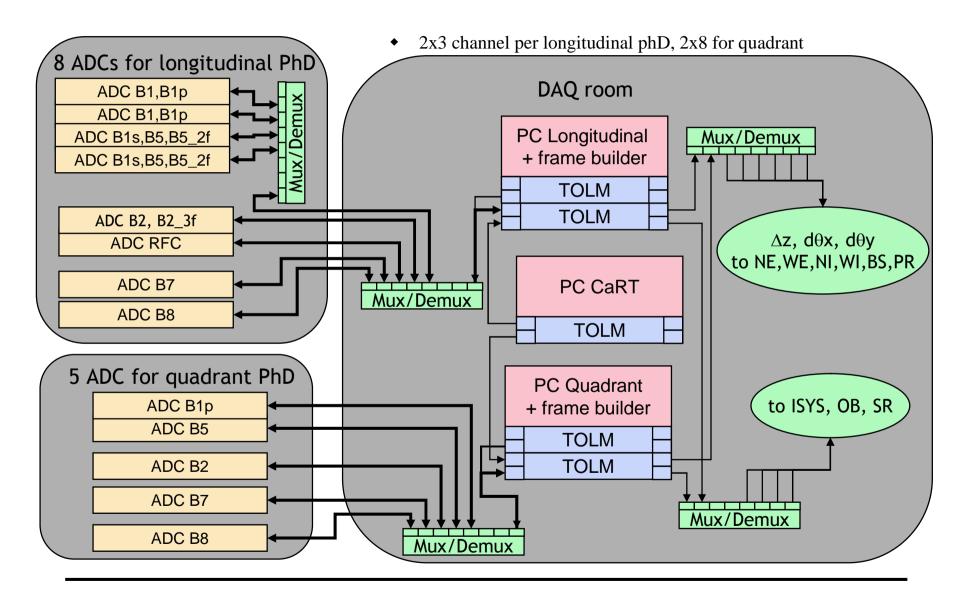




Virgo+ Online Architecture

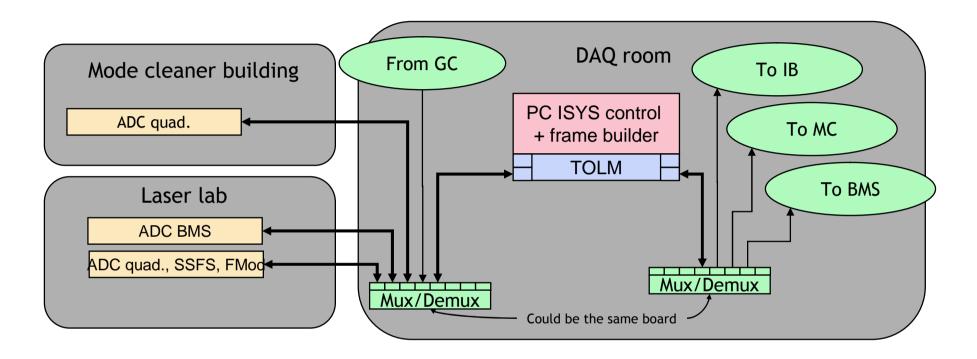


PR – GC, QR - GCAli



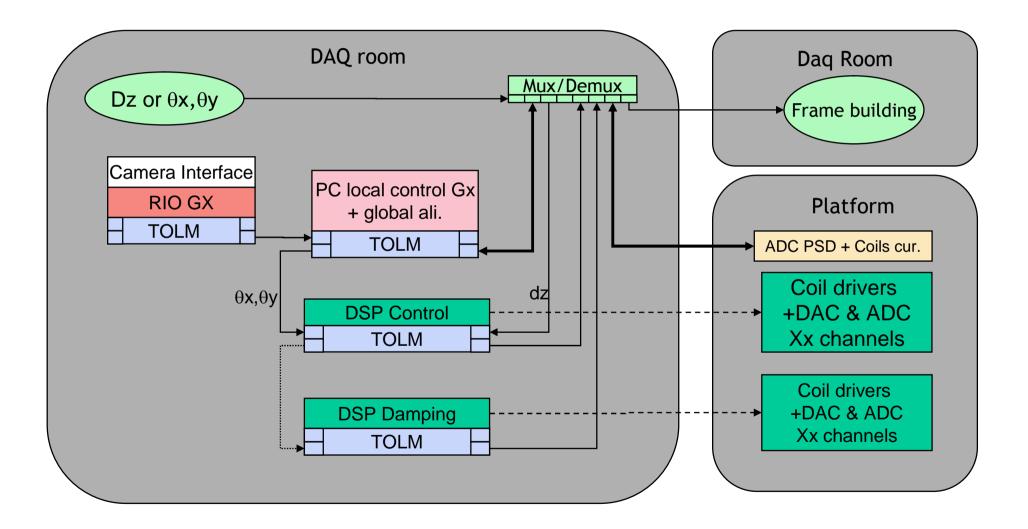


ISYS - Proposition



• The PC ISYS runs as ISYS controller









- Locking servers:
 - Scalable architecture to allow the Pr and Gc servers to run on the same or different PCs
 - Design almost complete
 - Keep the dictionary for the DAQ collection
 - Use the dictionary for the pipeline exchange
- The *TOLM* board is compatible with the RIO PCI architecture
 - The GxS server will still run on the RIO
 - The Detection slow control will be done at the first time on the RIO
 - No DAC with *TOLM* interface
- Timing:
 - The time stamp is directly available at the *TOLM* level as GPS time stamp
 - Push on each input packet by the *TOLM* (PCI, DSP link)
 - Timing library will be developed/upgraded



- TDB production and tests on July-August 2007
- TOLM
 - v1 production October-November2007
 - v2 production January-February2008
- MUX-DEMUX production and tests on September-October 2007
- ADC
 - Design complete First prototype expected the beginning of July2007
 - Final production foreseen on December2007-Fevrier2008
- TOLM DSP and Frame Builder : Integration test in September 2007
 - TOLM driver and libraries for Linux/Linux-RTAI
 - Dictionary
 - TOLM Frame builder
- TOLM Pr-GC servers: November 2007
- On site installation: May 2008