



Converter Design

Design Review, October 31, 2007

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Paul Schwinberg, Daniel Sigg,

Initial LIGO Limitations

- ❑ Collocation of analog and digital
 - Signals converge at converter nodes
- ❑ Limited timing support
 - Clock input only, no synchronization input, Rely on cycle count
- ❑ Poor noise performance
 - Sophisticated whitening & dewatering filters, switchable
- ❑ Inadequate throughput
 - VME bus latency limitations, 4 boards max.
- ❑ Convoluted data paths
 - Network topology grew over time, Reflective memory limitations
- ❑ High costs
 - Dependent on a single manufacturer

Requirements

□ Timing

- Absolute timing precision relative to UTC: $1\mu\text{s}$
- Guaranteed (no counting of cycles forever)
- Latency between converter and processor: $< 5\mu\text{s}$

□ Noise

- Converter range: $\pm 10\text{V}$ SE or $\pm 20\text{V}$ DE
- Converter noise: $100\text{--}300\text{nV}/\sqrt{\text{Hz}}$ (SE, best effort)
- No electrical connection between converters and processors (fiber)

□ Others

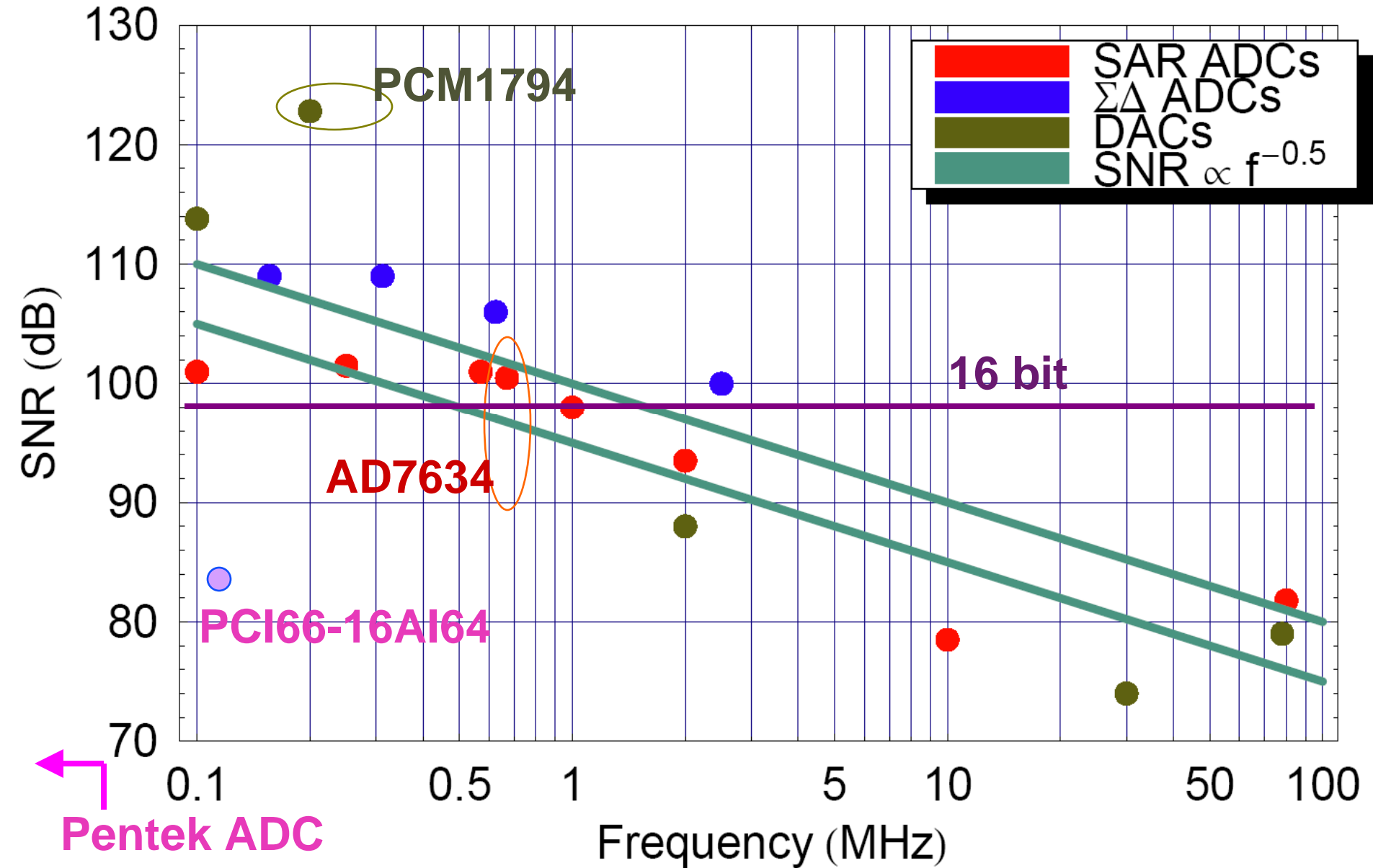
- No restriction on converter location
- Detection of transmission errors
- Support for diagnostics

State of Technology

- ❑ $\Sigma\Delta$ -Modulators
 - Typically paired with FIR filters, long delays
- ❑ SAR (Successive Approximation Register)
 - Analog Devices AD7634: 18 bit, 570 kHz, SNR 101 dB
- ❑ Advanced Segment
 - TI PCM1794A, 24 bit, 200 kHz, SNR 132 dB (A-weighted / $f_{\text{Nyquist}} \sim 12\text{kHz}$)
- ❑ Sweet spot around $\frac{1}{2}$ MHz sampling rate

$$\text{Noise} = \frac{FS_{pp}}{2\sqrt{2}} \times \frac{1}{SNR} \times \frac{1}{\sqrt{f_{\text{Nyquist}}}}$$

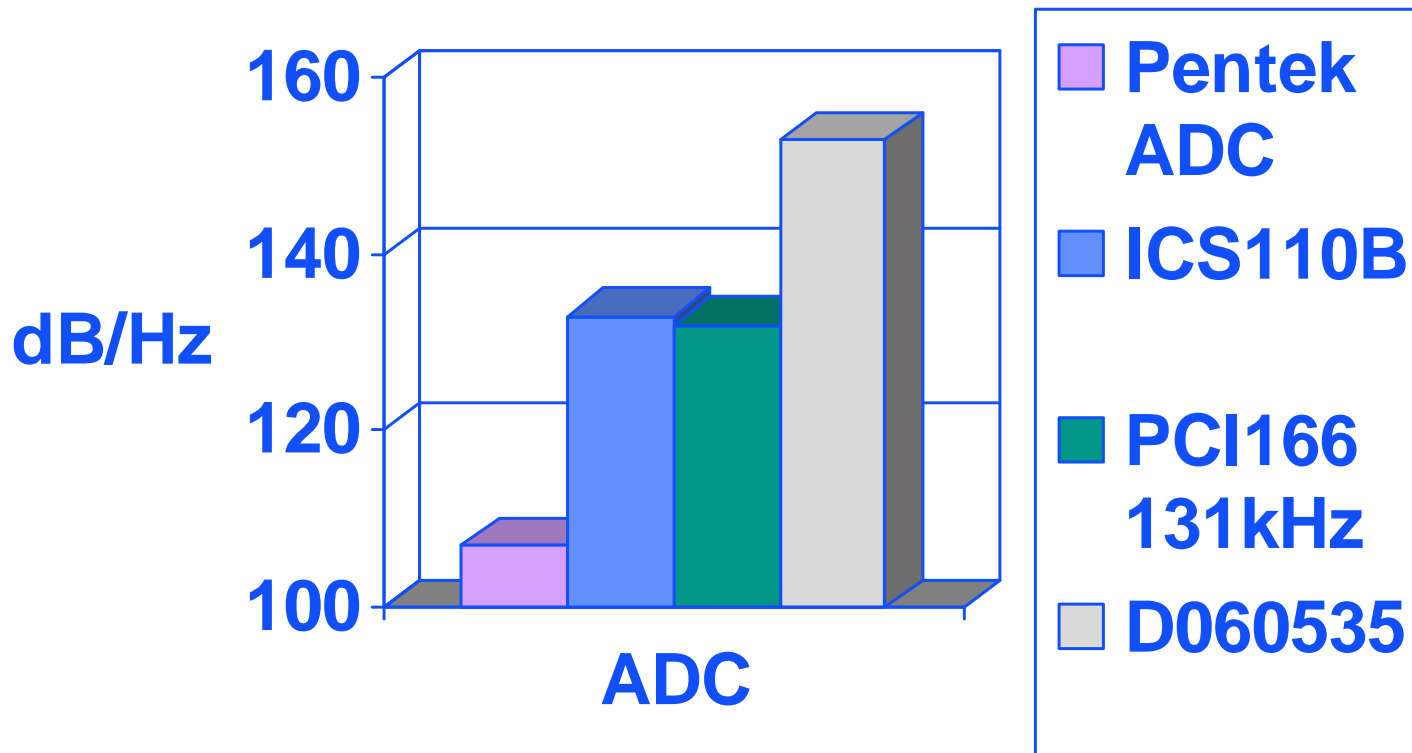
Converter Chart



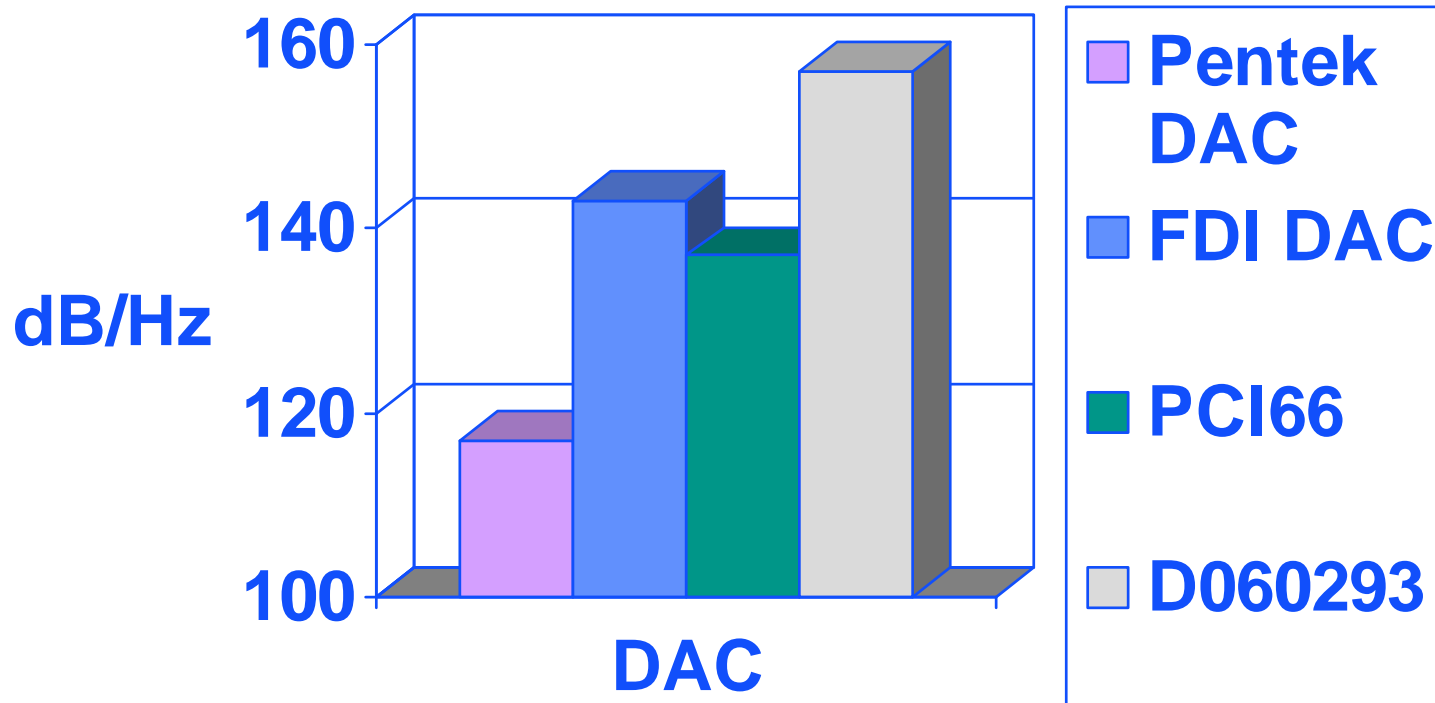
Comparison

Device	Noise	Range	Ratio	I/O	Price
Pentek 6102 ADC	15 $\mu\text{V}/\sqrt{\text{Hz}}$	10 Vpp	107 dB/Hz	8/8	8000
ICS-110B ($\Sigma\Delta$)	300 nV/ $\sqrt{\text{Hz}}$	4 Vpp	133 dB/Hz	32/0	10000
Pentek 6102 DAC	5 $\mu\text{V}/\sqrt{\text{Hz}}$	10 Vpp	117 dB/Hz	8/8	8000
FDI DAC	500 nV/ $\sqrt{\text{Hz}}$	20 Vpp	143 dB/Hz	0/8	8000
Commercial:					
PCI66-16AI64SSA (16kHz/131kHz)	10 $\mu\text{V}/\sqrt{\text{Hz}}$ 3.5 $\mu\text{V}/\sqrt{\text{Hz}}$	40 Vpp	123 dB/Hz 132 dB/Hz	32/0	3900
PCI66-16AO16	~ 1 $\mu\text{V}/\sqrt{\text{Hz}}$	20 Vpp	137 dB/Hz	0/16	3500
In-House:					
D060535 (ADC)	320nV/ $\sqrt{\text{Hz}}$	40 Vpp	153 dB/Hz	16/0	2000
D060293 (DAC)	~ 200 nV/ $\sqrt{\text{Hz}}$	40 Vpp	157 dB/Hz	0/16	2000

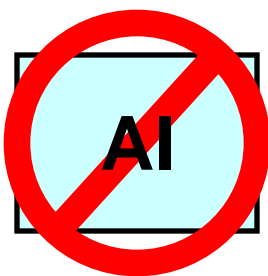
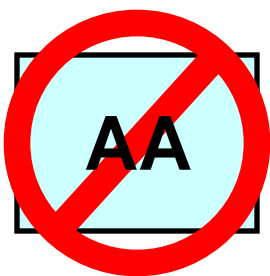
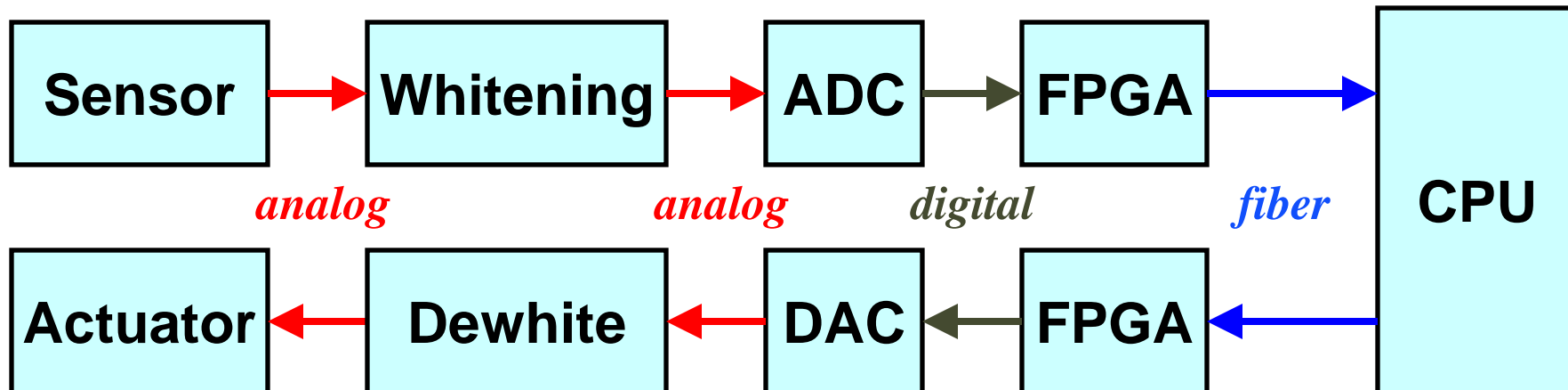
ADC Performance



DAC Performance



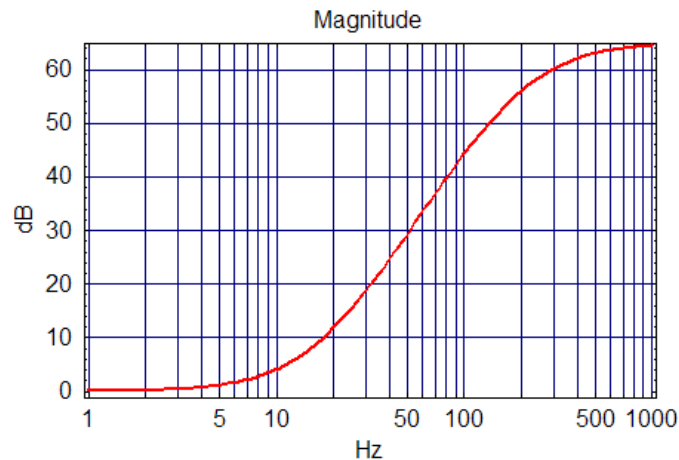
In-House System



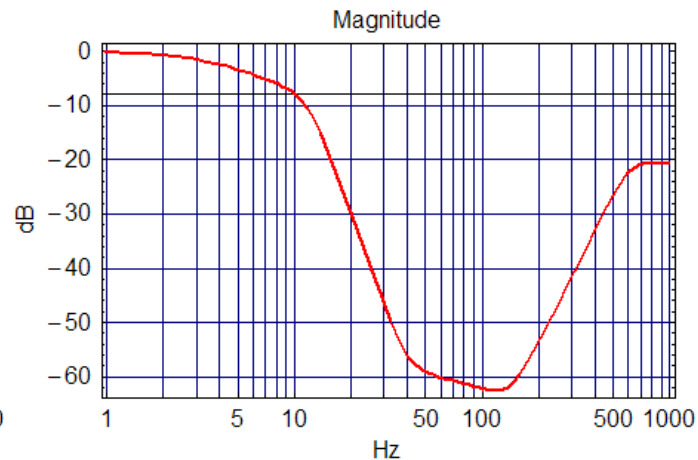
No Anti-Aliasing Boards
No Anti-Image Boards
Strongly Reduced Whitening
Reduced Dewhiting

Whitening/Dewhitening

- Compress the analog signal to fit the digital SNR



AS port whitening



Coil driver dewhitening

Pentek ADC → D060535: Win 45 dB!

FDI DAC → D060293: Win 10-20 dB

Integrated Timing

- ❑ Converter Clock
 - VCXO locked to timing receiver
 - FPGA clock & converter clock are the same
- ❑ Synchronization
 - 1 PPS signal from timing receiver
 - FPGA counters are synchronized by 1 PPS
- ❑ Data Transfer
 - Full time stamp on both send and receive
 - Sender deterministic
 - Receiver time stamp checked against allowed time interval

Timing is guaranteed in hardware!

ADC Board (D060535)

- ❑ 16 channels input
- ❑ Analog front-end
 - Fully differential, 40 Vpp
 - 5th order Cheby, 200kHz, 0.5dB ripple
- ❑ 524288 Hz sampling rate
- ❑ Analog Devices AD7634
- ❑ Onboard voltage regulators & reference
- ❑ LVDS interface to FPGA

Channel 1

Input

Channel 16

Regulators

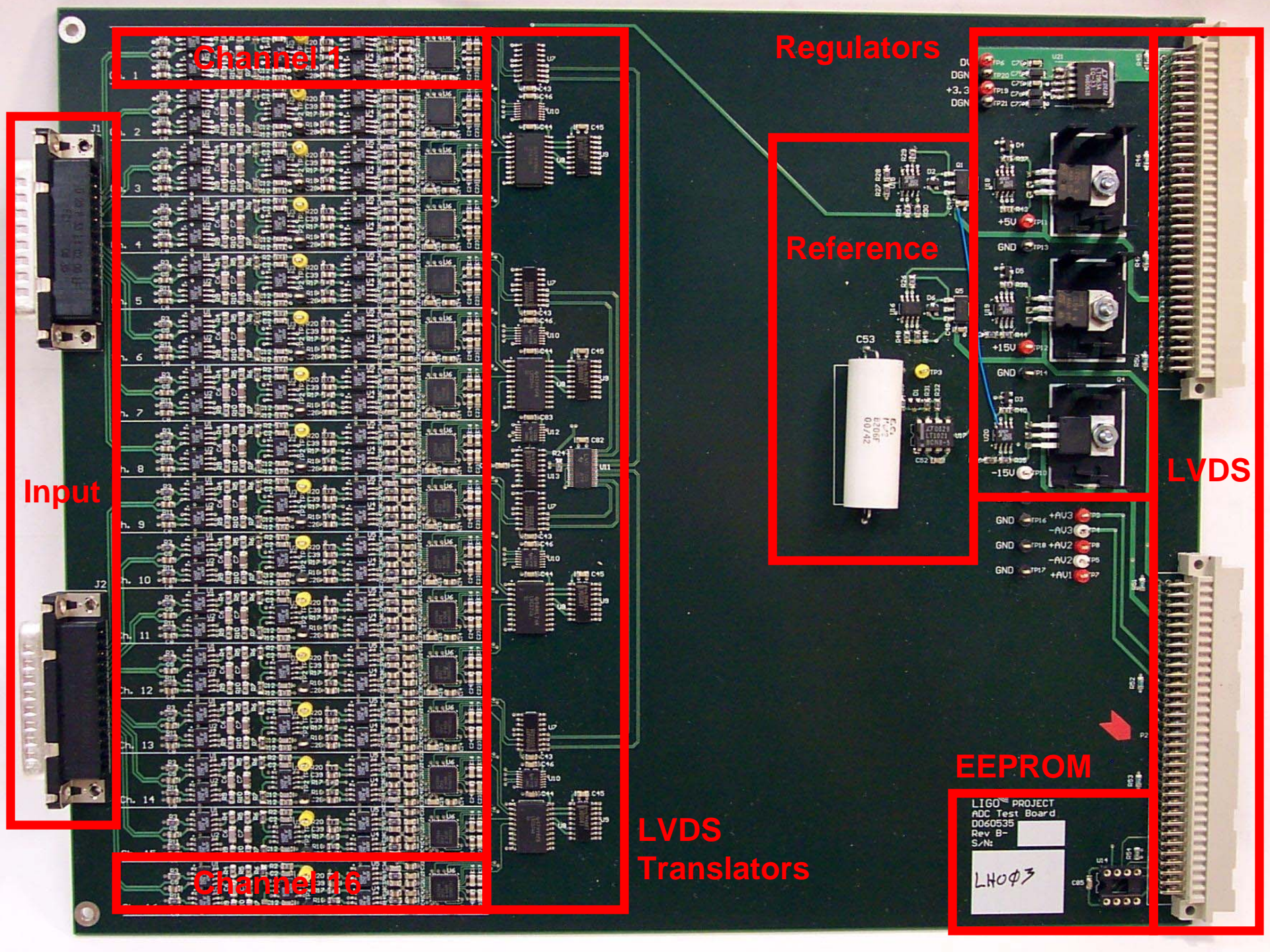
Reference

LVDS

EEPROM

LVDS Translators

LIGO PROJECT
 ADC Test Board
 DD60535
 Rev B-
 S/N: LH043



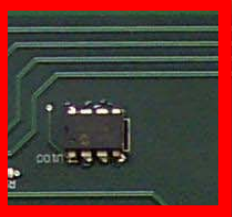
DAC Board (D060293)

- ❑ 16 channels output
- ❑ Analog front-end
 - Fully differential, 40 Vpp
 - 5th order Cheby, 53kHz, 0.1dB ripple
- ❑ 524288 Hz sampling rate (64 kHz bandwidth)
- ❑ Texas Instruments PCM1794A
- ❑ Onboard voltage regulators & reference
- ❑ LVDS interface from FPGA

LVDS

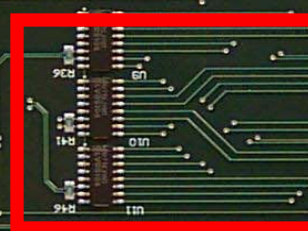


EEPROM

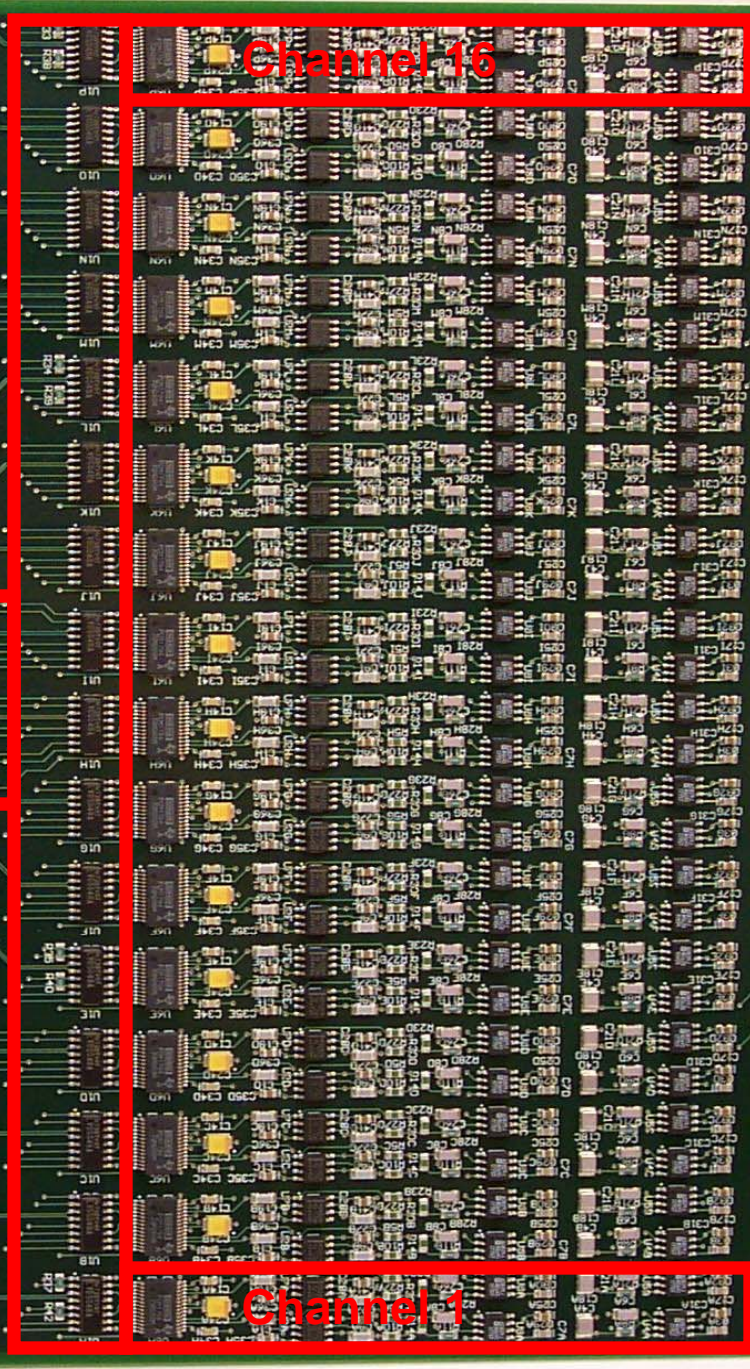
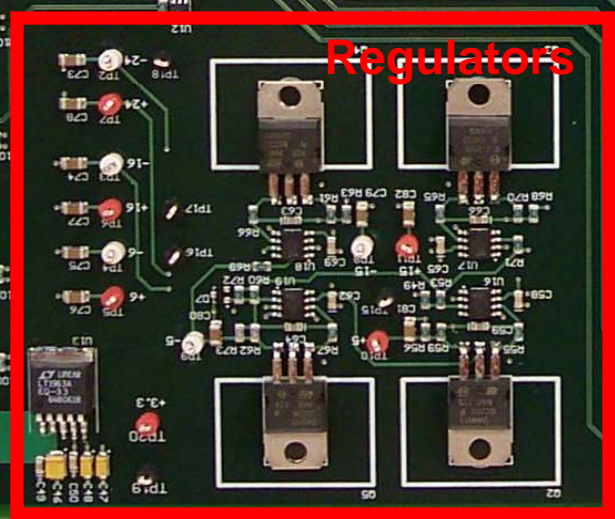


Reference

LVDS Translators



Regulators



Channel 16

Channel 1

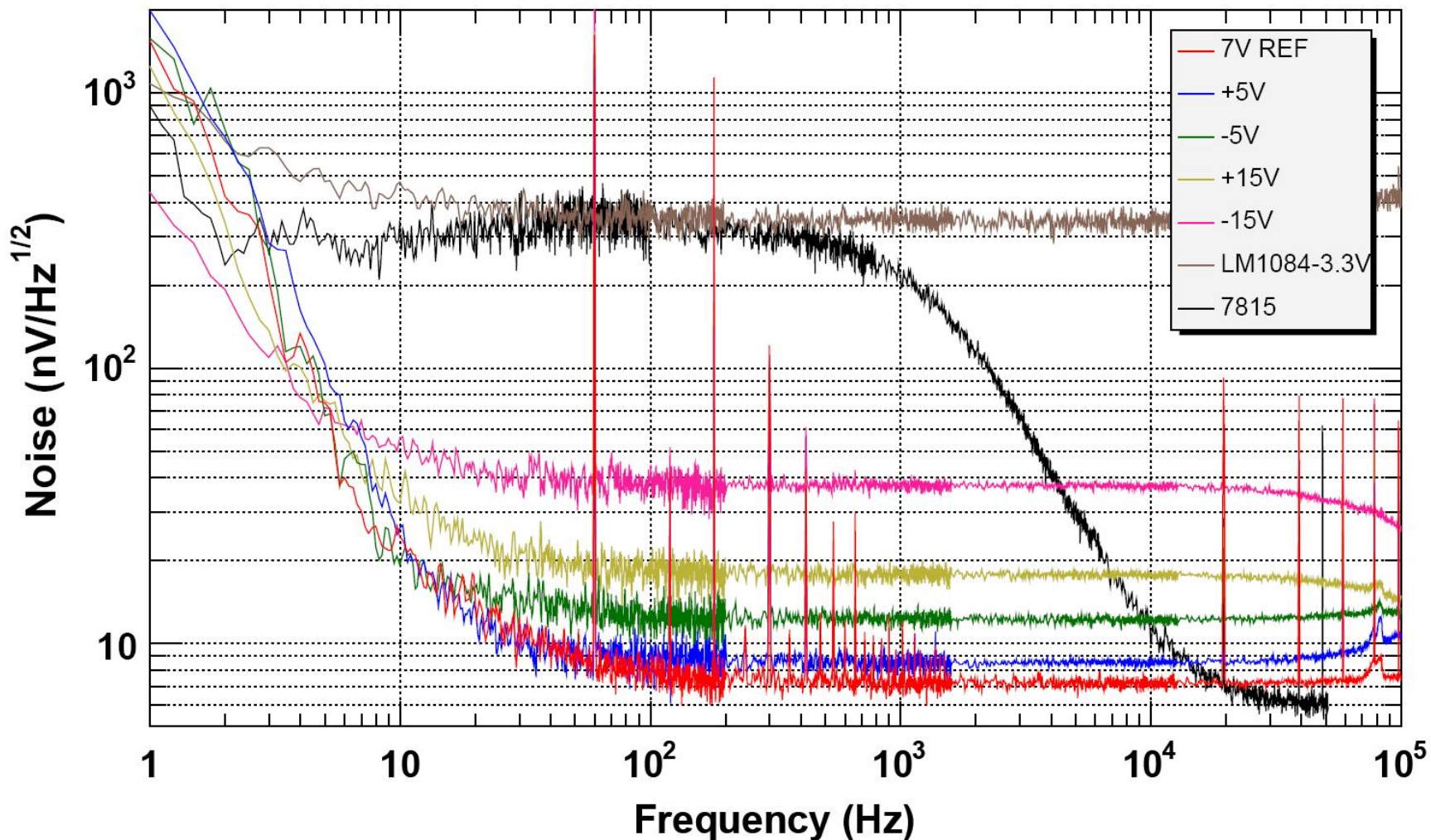


Output

L1G0
Rev A-
D06D293
D0C1794M
S/N6

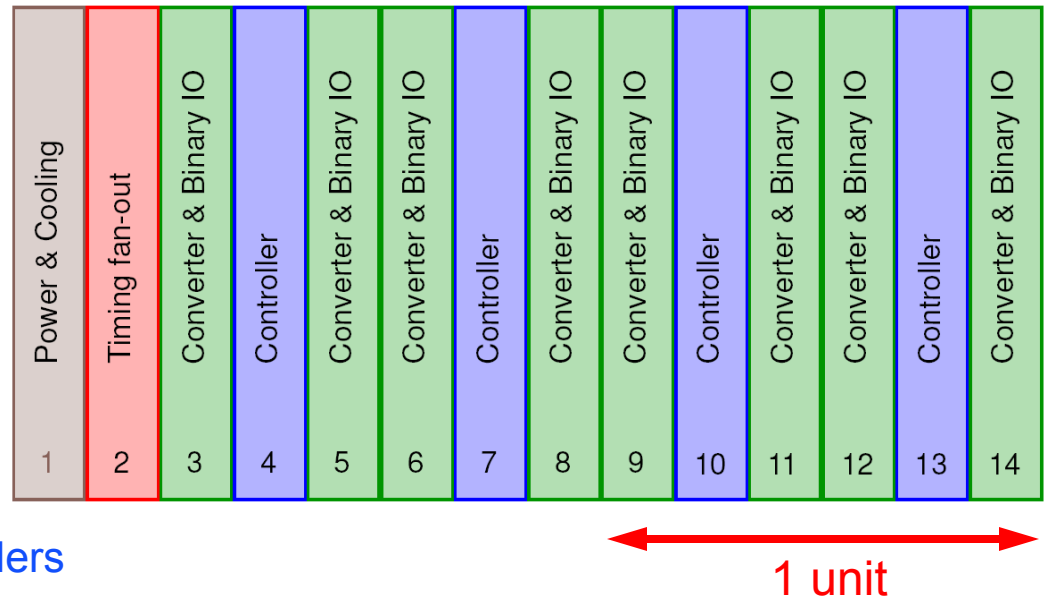
Low-Drop Low-Noise Voltage Regulators

Low Drop Power Regulators



Crate & Backplane

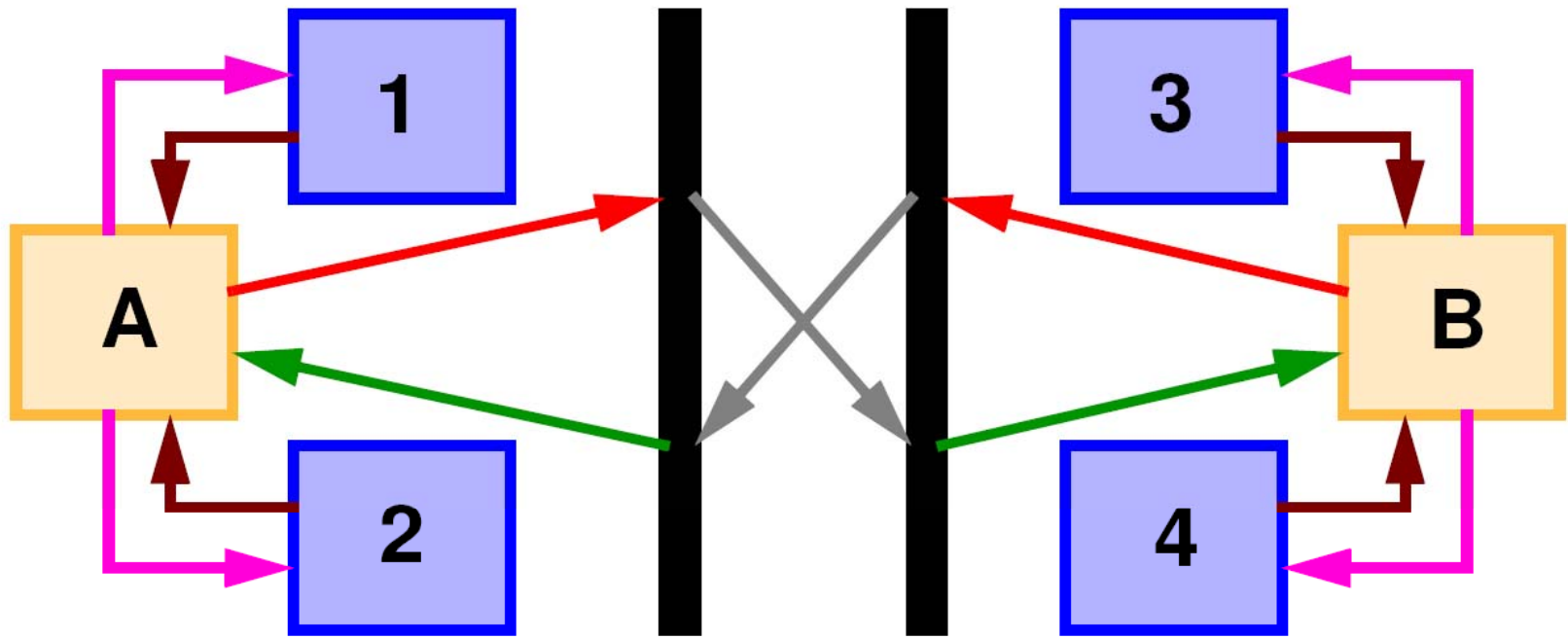
- ❑ Eurocrate IEEE 1101.1/1101.10
- ❑ 6U x 280mm x 6HP
- ❑ 2 converters per controller
- ❑ Connectors
 - VME type for converters
 - VME64X type for controllers
 - All connections are point-to-point (no bus)
- ❑ 1 unit = 2 controllers + 4 converters
- ❑ $\pm 16.5V$, $\pm 6.5V$ & $\pm 24V$ analog supplies
- ❑ 12V digital supply \rightarrow 5V & 3.3V digital



Controller Board

- ❑ Xilinx Spartan 3A DSP: XC3SD1800A (2x)
 - 37000 logic cells, 84 DSP slices, 1.5 MBit RAM
 - Converter control: clocks and serial interfaces (LVDS)
 - Filter Engines
 - Time-multiplexed serial links to uplink FPGA
- ❑ Xilinx Virtex 4FX: XC4VFX20
 - 2 x gigabit ethernet SFP transceivers & EMACs
 - Timing transceiver & logic
 - AES/EBU interfaces for mixed analog-digital testing
 - Digital IO lines
- ❑ Digital power supplies
 - 12V input to 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V & whatever
 - Multi-phase synchronous

Backplane Links



- Backplane
- Filter engine FPGA: 1 to 4
- Uplink FPGA: A and B

- Downstream link
- Upstream link
- Downstream clock and status
- Upstream half link

Filter Engine (1)

- Multiple second-order sections:

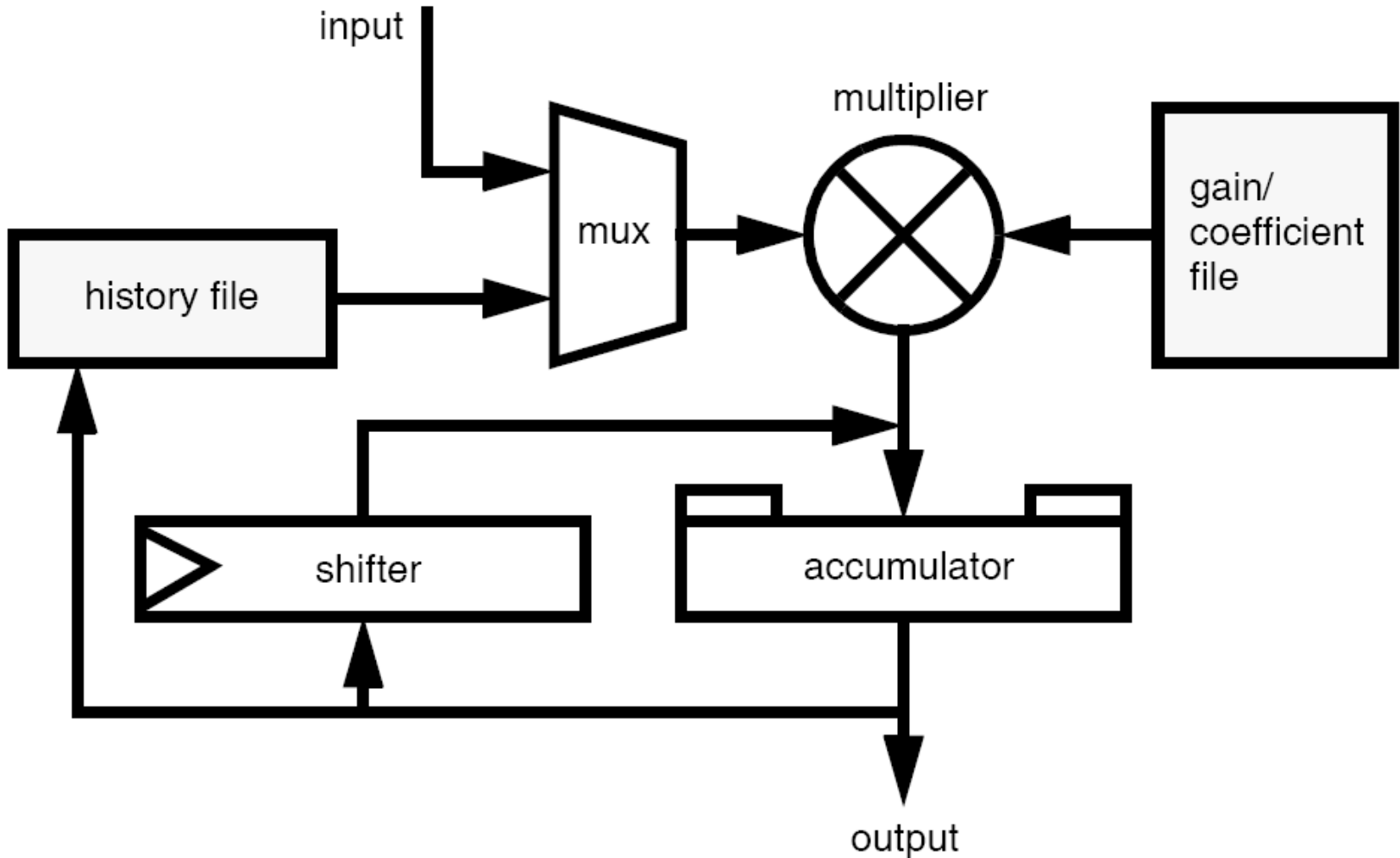
$$H(z) = g \prod_{k=1}^{N_s} \frac{c_{0k}(1 + b_{1k}z^{-1} + b_{2k}z^{-2})}{1 - a_{1k}z^{-1} - a_{2k}z^{-2}}$$

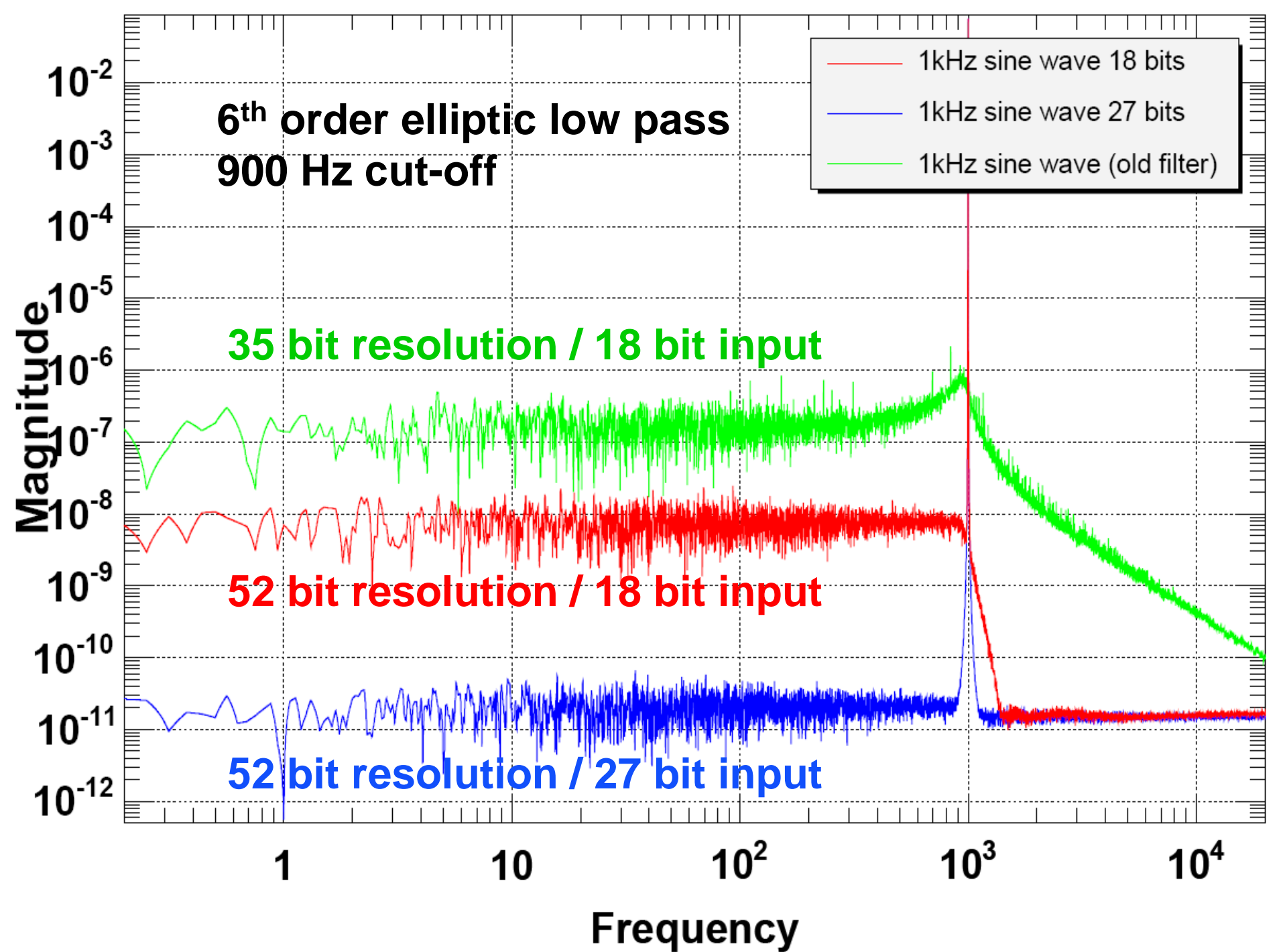
- Formula for a single SOS:

$$y_i = c_0(x_i + b_1x_{i-1} + b_2x_{i-2}) + a_1y_{i-1} + a_2y_{i-2}$$

- 4 multiplications with coefficients, old input and old output values
- 4 accumulations
- c_0 is a shift operation

Filter Engine (2)





ADC & DAC Performance

- Josh Myers G070604-B

Development Status

- ❑ ADC board
 - Prototype and testing done
 - Ready for production with small revisions
- ❑ DAC board
 - Prototype in hand
 - Testing in progress
- ❑ Controller board
 - Schematics done
 - Filter engine has been simulated and tested
 - Simulations for uplink code are underway
- ❑ Crate
 - Backplane defined
 - Thermal loading under investigation
 - Power supplies available as prototype

Development Plans

- ❑ Finished testing of DAC board
 - End of 2007, \$7000 if another revision is required
- ❑ Build and test controller board
 - Manufacturing by Dec 2007, testing by March 2008
 - Simulation models by Jan 2008
 - \$14000 (two revisions)
- ❑ Crate
 - Build backplane by Jan 2008, \$4000
 - Assemble prototype crate by Feb 2008, \$5000
- ❑ Integration
 - Testing with computer back-end by mid 2008, \$2000
 - Small production run for testing at LASTI, 40m, etc., \$56000
- ❑ Test stand for verification and automatic testing
 - Requires outside help, \$13000

Conclusions

- ❑ Highest performance ADC and DAC boards
- ❑ Fully integrated timing and synchronization
- ❑ Computer doesn't see oversampling
 - Works at 16384Hz and 2048Hz
 - Compute load at these frequencies shouldn't be a problem
- ❑ Design owned by us
 - No dependency on single board manufacturer
 - Person power for in-house development & testing required
- ❑ Clear path for future extensions and upgrades
- ❑ Good reasons for adopting this system as the new baseline