aLIGO ISC Whitening Chassis Test Outline
LIGO-T1100291-v1
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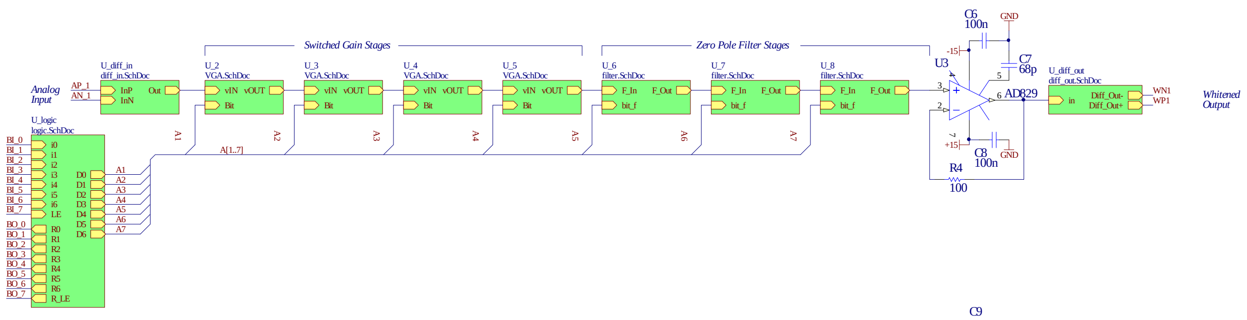
1. Overview

1.1. Testing Scope - This test procedure applies to ISC Whitening Filter circuit board D1001530-v4, two of which are contained within chassis assembly D1002559. D1002559 is a remotely configurable 8-channel general purpose whitening filter bank. This test procedure provides instructions for performance verification for the entire assembled chassis.

1.2. Block diagram

Figure 1



2. Testing

2.1. Assumptions

2.1.1. Each whitening chassis requires a total of 64 individual parallel control lines (bits) to control all the gain and filter combinations. While this is possible to do with external switches or jumpers, it is far more efficient to test this chassis using an automated binary control chassis such as the Acromag 384 channel binary interface module D1100251.

2.1.2. Each production chassis must be functionally tested according to the procedure in this document. The test results are to be recorded using the form Fxxx. The completed form is to be loaded in the DCC, in the chassis' S-number file card.

2.1.3. For most measurements taken during this procedure, signals will be input and read from connectors on the front and rear of the chassis under test. This convention yields the best overall test of functionality.

2.1.4. The person using this procedure is familiar with Dynamic Signal Analyzers and rudimentary test equipment including oscilloscopes, power supplies, and multimeters.

2.2. Front and rear panel layout

Figure 2, ISC Whitening Chassis Front Panel

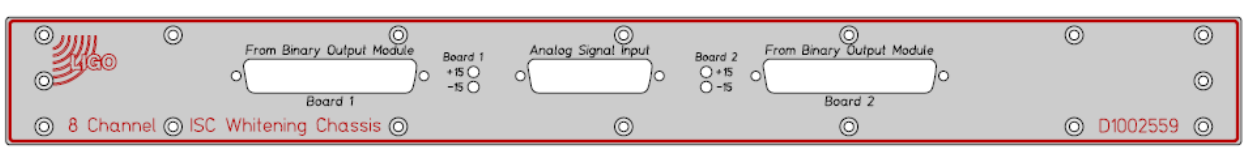
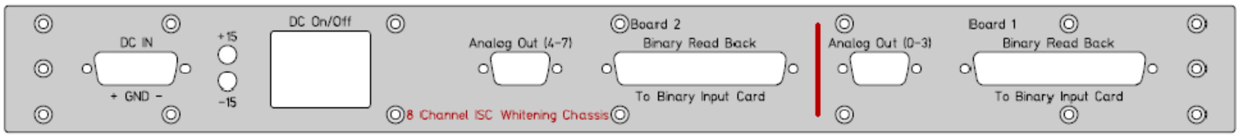


Figure 3, ISC Whitening Chassis Rear Panel



2.3. Unit Identification

2.3.1. Serial numbers for the chassis, both main filter boards and the DC power regulator board must be recorded. It is not required to record data on the front panel interface circuit board as this will not be serialized.

2.4. DC Power Supply Tests

2.4.1. Apply +/- 18, +/-200 mV Volts DC to the chassis under test and record front and rear panel LED operation, total positive and negative power supply current, internal regulator output voltage and individual circuit board power supply currents as required in Fxxx

2.5. Transfer Function Tests

2.5.1. Using an SR785 (or automated test setup), take a transfer function for each of the 8 channels associated with the front panel Analog Signal Input and rear panel Analog Out connectors as shown in Table 1.

Table 1

Front Panel Analog Input		Rear Panel Analog Out (0-3)	Rear Panel Analog Out (4-7)
Pin	**Function**	**Pin**	**Pin**
1 and 14	Chan. 0 +/-	1 and 6	
2 and 15	Chan. 1 +/-	2 and 7	
3 and 16	Chan. 2 +/-	3 and 8	
4 and 17	Chan. 3 +/-	4 and 9	
5 and 18	Chan. 4 +/-		1 and 6
6 and 19	Chan. 5 +/-		2 and 7
7 and 20	Chan. 6 +/-		3 and 8
8 and 21	Chan. 7 +/-		4 and 9

2.5.2. Repeat the tests for every possible permutation of gain and filter choice. Needs elaboration (frequency range, signal levels, etc.).

2.6. Noise Tests

2.6.1. Using an SR785 (or automated test setup), differentially measure the output noise for each of the 8 analog outputs present on the two real panel d-subminiature connectors. The front panel analog inputs should be shorted to ground during this measurement (this is most easily accomplished by making a shorting jig out of a mating 25 pin D-sub connector).

2.6.2. Repeat the noise tests for each permutation of gain and filter function.

2.7. Expected Noise Performance – The following tables detail the expected noise performance for different combinations of whitening gain and filters.

Table 2

Gain State	Measured Output Noise @1Hz (dBVrms/√Hz)	Measured Output Noise @10Hz (dBVrms/√Hz)	Measured Output Noise @100Hz (dBVrms/√Hz)	Gain at 1Hz (dB)	Gain at 10Hz (dB)	Gain at 100Hz (dB)
0dB	-134	-145	-150	0	0	0
3dB	-133	-145	-150	3	3	3
6dB	-132	-143	-146	6	6	6
12dB	-128	-137	-141	12	12	12
24dB	-120	-127	-130	24	24	24
45dB (all DC gain)	-97	-106	-107	45	45	45
1st Filter only	-130	-133	-133	2.9	17	20
1st & 2nd Filter	-123	-115	-112	5.9	34	40
1st, 2nd & 3rd Filter	-116	-98	-91	8.8	51	60
Everything On	-87	-55	-48	53.9	96.2	105

Table 3

Gain State	Calculated Input Noise @1Hz (nVrms/√Hz)	Calculated Input Noise @10Hz (nVrms/√Hz)	Calculated Input Noise @100Hz (nVrms/√Hz)
0dB	200	56	32
3dB	158	40	22
6dB	126	35	25
12dB	100	35	22
24dB	63	28	20
45dB (all DC gain)	79	28	25
1st Filter only	226	32	22
1st & 2nd Filter	359	35	25
1st, 2nd & 3rd Filter	575	35	28
Everything On	90	28	22

Table 4 Whitening Chain with AD829 Amplifiers

Gain State	Measured Output Noise @1Hz (dBVrms/√Hz)	Measured Output Noise @10Hz (dBVrms/√Hz)	Measured Output Noise @100Hz (dBVrms/√Hz)	Gain at 1Hz (dB)	Gain at 10Hz (dB)	Gain at 100Hz (dB)
0dB	-134	-145	-150	0	0	0
3dB	-133	-145	-150	3	3	3
6dB	-132	-143	-146	6	6	6
12dB	-128	-137	-141	12	12	12
24dB	-120	-127	-130	24	24	24
45dB (all DC gain)	-97	-106	-107	45	45	45
1st Filter only	-130	-133	-133	2.9	17	20
1st & 2nd Filter	-123	-115	-112	5.9	34	40
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0dB	200	56	32
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