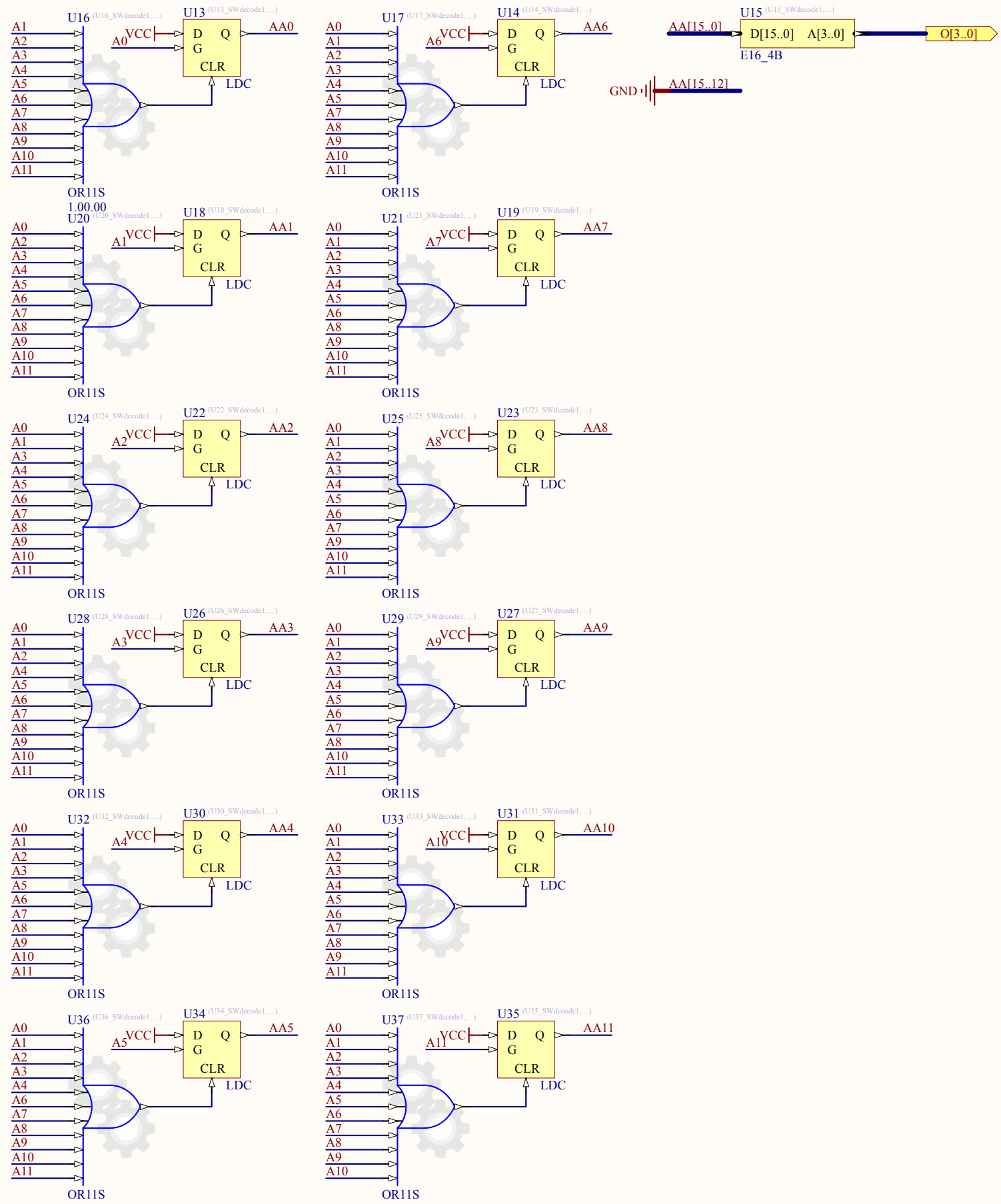


Title		
RF AM Stabilization CPL		
Size	Number	Revision
B	D0900761	A
Date:	7/10/2015	Sheet 1 of 2
File:	C:\Users\daniel\Documents\EOMDriverControlCPL1.SchDoc Drawn By: Daniel Sigg	

A[11.0] A[11.0]



Title		
RF AM Stabilization CPL		
Size	Number	Revision
B	D0900761	A
Date:	7/10/2015	Sheet 2 of 2
File:	C:\Users\...EOMDriverControlCPL2.SchDoc Drawn By: Daniel Sigg	

```
-----
-- SubModule EOMDriverControlCPL3
-- Created 4/27/2009 3:32:35 PM
-----
```

```
Library IEEE;
```

```
Use IEEE.Std_Logic_1164.all;
```

```
Use IEEE.Numeric_Std.all;
```

```
entity EOMDriverControlCPL3 is port
```

```
(
  A      : in   std_logic_vector(7 downto 0);
  D      : out  std_logic_vector(15 downto 0)
);
```

```
end EOMDriverControlCPL3;
```

```
-----
architecture Structure of EOMDriverControlCPL3 is
```

```
-- Type Declarations
```

```
type word is range 0 to 65535;
```

```
type rom_type is array (0 to 255) of word;
```

```
-- constant Declarations
```

```
constant rom : rom_type :=
```

```
--( 3772, 3857, 3938, 4024, 4112,
(4201, 4295, 4392, 4496, 4593, 4693,
4798, 4907, 5019, 5139, 5250, 5370, 5495, 5623, 5755, 5887, 6021,
6159, 6307, 6455, 6605, 6758, 6921, 7084, 7254, 7423, 7602, 7780,
7965, 8156, 8341, 8547, 8753, 8961, 9169, 9390, 9612, 9840, 10079,
10319, 10566, 10822, 11082, 11347, 11620, 11899, 12181, 12472, 12775,
13080, 13400, 13721, 14052, 14386, 14732, 15089, 15456, 15818, 16212,
16590, 16995, 17401, 17821, 18260, 18697, 19148, 19608, 20073, 20563,
21048, 21568, 22087, 22613, 23166, 23717, 24287, 24875, 25470, 26071,
26700, 27341, 28013, 28677, 29368, 30075, 30807, 31533, 32268, 33052,
33849, 34661, 35489, 36344, 37211, 38118, 39028, 39960, 40920, 41899,
42925, 43976, 45016, 46093, 47210, 48367, 49542, 50727, 51935, 53189,
54449, 55803, 57129, 58540, 59960, 61450, 62900, 64400, others =>4201);
```

```
-- Functions
```

```
function get_word (r : in rom_type; i : natural) return natural is
  variable c : word;
begin
  c := r (i);
  return natural(c);
end function get_word;
```

```
-- Signal Declarations
```

```
signal addr : unsigned (7 downto 0);
signal DD : std_logic_vector(15 downto 0);
```

```
begin
```

```
addr <= unsigned (A);
DD <= std_logic_vector (To_unsigned (get_word (rom, To_integer (addr)), 16));
D(14 downto 0) <= DD(14 downto 0);
D(15) <= not DD(15);
```

```
end Structure;
```