

<i>Title</i>	<i>ITM Low Voltage ESD Driver Chassis Test Procedure</i>
<i>Author</i>	<i>R. Abbott, Caltech</i>
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<i>Hardware Version</i>	<i>PCB D160012-v12 in Chassis D1600092</i>

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## 1 Overview

This procedure is used to verify proper operation of the D1600092, ITM Low Voltage Low Noise ESD Driver Chassis. This chassis operates at voltages up to 430VDC and portions of this procedure assume that the person performing the test is familiar with high voltage circuit testing. **The Test Technician or Engineer MUST be a LIGO approved Qualified Electrical Worker specifically authorized to work on energized equipment to perform high voltage measurements on exposed equipment.**

**Table 1**

<b>Chassis Serial Number</b>		
<b>Main Board Serial Number</b>		
<b>Date</b>		
<b>Tested By</b>		
<b>Overall Test Result</b>	PASS	FAIL
	<input type="checkbox"/>	<input type="checkbox"/>

## 2 DC Measurements Section

### 2.1 Quiescent current draw

For the sake of safety, **DO NOT APPLY HIGH VOLTAGE TO THE HIGH VOLTAGE POWER CONNECTOR ON THE REAR PANEL UNTIL PROMPTED.** The high voltage transfer function and output noise will be done in the last section of this procedure.

External to the chassis under test, sequentially insert a Fluke Multi-meter in series with each power form in the table below and measure the power supply current. Record the results in the following table. Mark each measurement as Pass or Fail. Remove meter after completion of the quiescent current measurements.

**Table 2 Quiescent Current Draw and Regulated Voltages**

<b>Quiescent Current/Voltage</b>	<b>Specified Value</b>	<b>Measured Value</b>	<b>Pass</b>	<b>Fail</b>
+18V Supply	230mA +/- 20mA		<input type="checkbox"/>	<input type="checkbox"/>
-18V Supply	-210mA +/- 20mA		<input type="checkbox"/>	<input type="checkbox"/>
+15V Supply (internal)	14.8VDC +/- 200mV		<input type="checkbox"/>	<input type="checkbox"/>
-15V Supply (internal)	-15.0VDC +/- 200mV		<input type="checkbox"/>	<input type="checkbox"/>
+V (+24V) Supply	20mA +/- 10mA		<input type="checkbox"/>	<input type="checkbox"/>
-V (-24V) Supply	-20mA +/- 10mA		<input type="checkbox"/>	<input type="checkbox"/>

### 3 PI Path Main Signal Chain

A signal applied to the “Drive Inputs from DAC” connector on the front panel propagates through the High-pass Filter stage (10 kHz) and eventually emerges at the front panel SHV connectors labeled “To ITM” for each respective quadrant.

In the following section, the transfer function will be taken of the main PI signal path. Use an SR785 dynamic signal analyzer to obtain the transfer function over the frequency ranges identified in the following data tables. Mark each test as PASS or FAIL as appropriate.

Apply a signal to the front panel connector labeled “Drive Inputs from DAC” according to the following pin map. The output for each measurement will be taken from the associated SHV connector indicating “To ITM” for that function:

**Table 3, DAC Input Pin Map**

<b>Pin (+,-)</b>	<b>Function</b>
1,9	Bias Path Input
2,10	UR Path PI Input
3,11	LR Path PI Input
4,12	UL Path PI Input
5,13	LL Path PI Input
6,14	LF DC Input

**Table 4, Main Path Transfer Function**

<b>Function</b>	<b>Gain at 1 kHz</b>	<b>Phase at 1 kHz</b>	<b>Gain at 20 kHz</b>	<b>Phase at 20 kHz</b>	<b>Pass</b>	<b>Fail</b>
<b>UR PI Path</b>	-45.1dB +/- 1dB	-116 +/- 3 deg.	5.1dB +/- 3dB	52 +/- 5 deg.	<input type="checkbox"/>	<input type="checkbox"/>
<b>LR PI Path</b>	-45.1dB +/- 1dB	-116 +/- 3 deg.	5.1dB +/- 3dB	52 +/- 5 deg.	<input type="checkbox"/>	<input type="checkbox"/>
<b>UL PI Path</b>	-45.1dB +/- 1dB	-116 +/- 3 deg.	5.1dB +/- 3dB	52 +/- 5 deg.	<input type="checkbox"/>	<input type="checkbox"/>
<b>LL PI Path</b>	-45.1dB +/- 1dB	-116 +/- 3 deg.	5.1dB +/- 3dB	52 +/- 5 deg.	<input type="checkbox"/>	<input type="checkbox"/>

## 4 Low Frequency DC Path Bit Control and Transfer Function

### 4.1 Binary Control and Monitoring

The Low Frequency DC path (LF DC) consists of a single input from a DAC that can fan out to each quadrant. Individual bit control allows each quadrant to be switched on or off independently. This path also has a single switchable dewhitening pole-zero stage. The state of the dewhitening stage is set by an individual bit control “PoleZeroByp” as outlined in the table below. The binary control input (rear panel 9-pin D-sub) is labeled “Binary Input”. A dedicated readback of the bit control is provided via a 9-pin D-sub connector on the rear panel labeled “Binary Monitor”. Mark the box “Pass or Fail” as appropriate after verifying each readback per the table below.

**Table 5**

<b>Function</b>	<b>Binary Input Pin</b>	<b>Effect of shorting Binary Input Pin to pin 5 (GND) of Binary Input D-sub</b>	<b>Associated Binary Monitor Output Pin</b>	<b>Binary Monitor State with respective Binary Input shorted</b>	<b>Pass</b>	<b>Fail</b>
UR LF DC Control	2	Path is NOT connected to respective front panel SHV connector	2 wrt 5	0V wrt 5	<input type="checkbox"/>	<input type="checkbox"/>
LR LF DC Control	7	Path is NOT connected to respective front panel SHV connector	7 wrt 5	0V wrt 5	<input type="checkbox"/>	<input type="checkbox"/>
UL LF DC Control	1	Path is NOT connected to respective front panel SHV connector	1 wrt 5	0V wrt 5	<input type="checkbox"/>	<input type="checkbox"/>
LL LF DC Control	6	Path is NOT connected to respective front panel SHV connector	6 wrt 5	0V wrt 5	<input type="checkbox"/>	<input type="checkbox"/>
Pole Zero Bypass	3	Pole-zero stage IS active	3 wrt 5	0V wrt 5	<input type="checkbox"/>	<input type="checkbox"/>

## 4.2 LF DC Path Transfer Function

This section verifies the transfer function of LF DC path and the monitoring amplifiers associated with each quadrant's output. Using an SR-785, observe the transfer function as prompted by the following table and mark each result as "Pass" or "Fail" as appropriate. The outputs are taken differentially at the front panel monitoring port labeled "Monitor Outputs to ADC".

**Table 6**

Input	Binary Input Pin State	Mag/Phase at 10Hz measured differentially at respective monitor output	Mag/Phase at 1 kHz measured differentially at respective monitor output	Function Tested	Pass	Fail
DAC Input Pins 6/14	All Open	Open, no connection seen to any monitor output	Open, no connection seen to any monitor output	All	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 6/14	2 and 3 to 5 shorted	20.3+/-1dB, -119.0 +/- 5 degrees at front panel monitor connector, pins 1,9	22.3+/-1dB, 44.7 +/- 5 degrees at front panel monitor connector, pins 1,9	UR LF DC	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 6/14	7 and 3 to 5 shorted	20.3+/-1dB, -119.0 +/- 5 degrees at front panel monitor connector, pins 2,10	22.3+/-1dB, 44.7 +/- 5 degrees at front panel monitor connector, pins 2,10	LR LF DC	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 6/14	1 and 3 to 5 shorted	20.3+/-1dB, -119.0 +/- 5 degrees at front panel monitor connector, pins 3,11	22.3+/-1dB, 44.7 +/- 5 degrees at front panel monitor connector, pins 3,11	UL LF DC	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 6/14	6 and 3 to 5 shorted	20.3+/-1dB, -119.0 +/- 5 degrees at front panel monitor connector, pins 4,12	22.3+/-1dB, 44.7 +/- 5 degrees at front panel monitor connector, pins 1,9	LL LF DC	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 6/14	6 to 5 shorted	33.4+/-1dB, -52.8 +/- 5 degrees at front panel monitor connector, pins 4,12	49.4+/-1dB, 47+/- 5 degrees at front panel monitor connector, pins 4,12	LL Pole-zero Bypass	<input type="checkbox"/>	<input type="checkbox"/>

## 5 Output Noise Measurements of Quadrant Drives

The output noise is measured with each respective PI and LF DC input shorted together and to ground. Use an SR-785 Signal Analyzer to measure the differential output voltage noise at each front panel monitor output per the table below. Mark each test as “Pass” or “Fail” as appropriate.

Table 7

Output	Binary Input Pin State	Noise at 20Hz measured differentially at respective monitor output	Noise at 100Hz measured differentially at respective monitor output	Noise at 20 kHz measured differentially at respective monitor output	Pass	Fail
UR Monitor Pins 1,9	2 and 3 to 5 shorted	3.9+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	12.5+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	40+/-5 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>
LR Monitor Pins 2,10	7 and 3 to 5 shorted	3.9+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	12.5+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	40+/-5 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>
UL Monitor Pins 3,11	1 and 3 to 5 shorted	3.9+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	12.5+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	40+/-5 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>
LL Monitor Pins 4,12	6 and 3 to 5 shorted	3.9+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	12.5+5,-1 $\mu\text{V}/\sqrt{\text{Hz}}$	40+/-5 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>

## 6 High Voltage Amplifier Transfer Function and Noise

The bias path of the ITM ESD Driver is powered by +/-430VDC supplies. The exposed high voltages present inside the chassis require that the chassis lid be in place prior to performing this portion of the test procedure, so **PUT THE CHASSIS LID ON BEFORE CONTINUING IN THIS TEST PROCEDURE**.

### 6.1 Bias Path Transfer Function and noise overview

The high voltage amplifier in the bias section of the ITM ESD Driver consists of an APEX PA-95 in an inverting configuration. The quiescent current draw for this part is 1.6mA per supply. In addition, the PA-95 output load is 399.9k $\Omega$  for the monitor divider in parallel with 500k $\Omega$  for the feedback resistors. This results in an equivalent resistive load of 222k $\Omega$ . The total power supply current can be calculated from these two parameters. With the lid on the chassis under test, apply the +/-18V and +/-24V supplies, then apply +/-430 to the high voltage power supply feed on the back of the chassis. Additionally, a multi-pole high voltage low pass filter is present on the output of the PA-95 to reduce bias path noise.

For the Bias path transfer function and noise measurements direct connection to the HV output SHV connector will destroy the SR-785. A suitable AC coupling unit must be built out of parts rated for the full 400V output of this amplifier chain. A 3 $\mu\text{F}$ , 700VDC capacitor mounted inside a metal box would be suitable (see DigiKey part number BC2786-ND). To further preclude against damage, a pair of 1N4001 silicon diodes should be used to form a bipolar voltage clamp such that rapid changes in voltage are limited at the SR-785 input. See the picture below for one such implementation.

**Figure 1, AC Coupling Box**

With the input to the SR-785 Dynamic Signal Analyzer AC coupled, the use of the above AC coupling box in conjunction with the 1 $\mu$ F capacitor and 1M $\Omega$  resistor internal to the SR-785, a 0.2Hz pole results. For measurements of 10Hz and above, this should prove insignificant.

## 6.2 Bias Path Transfer Function Measurement

With all chassis power supplies at the nominal voltage AND the lid on the chassis, use the AC coupling box to measure the transfer function of the bias path per the instructions in the table below.

**Table 8**

Input	Output	Mag/Phase at 10Hz	Pass	Fail
DAC Input Pins 1/9	Front Panel SHV "Bias to ETM" (USE AC Coupler Box)	1.2+/-1dB, 29.5 +/- 5 degrees at front panel SHV "Bias to ETM"	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 1/9	Front panel "Monitor Outputs to ADC" pins 5/13	6+/-1dB, 180 +/- 5 degrees at front panel monitor connector, pins 5/13	<input type="checkbox"/>	<input type="checkbox"/>

## 6.1 Bias Path Noise Measurement

With the conditions established per the table below, measure the output noise with the AC coupling box at the SHV front panel output. Use a well filtered, low voltage noise source to drive the DAC input where appropriate to avoid introducing noise. Mark each result “Pass” or “Fail” as appropriate

**Table 9**

<b>Input</b>	<b>Output</b>	<b>Noise at 100Hz</b>	<b>Noise at 1 kHz</b>	<b>Pass</b>	<b>Fail</b>
DAC Input Pins 1/9 shorted together and grounded	Front Panel SHV “Bias to ETM” (USE AC Coupler Box)	16 +/-3 nV/ $\sqrt{\text{Hz}}$	16 +/-3 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 1/9 driven to +10V	Front Panel SHV “Bias to ETM” (USE AC Coupler Box)	16 +/-3 nV/ $\sqrt{\text{Hz}}$	16 +/-3 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>
DAC Input Pins 1/9 driven to -10V	Front Panel SHV “Bias to ETM” (USE AC Coupler Box)	16 +/-3 nV/ $\sqrt{\text{Hz}}$	16 +/-3 nV/ $\sqrt{\text{Hz}}$	<input type="checkbox"/>	<input type="checkbox"/>