

DARM OLG TF (or CLG TF) Measurement

IN2 and/or EXC are stored into frames at T=0

61 μ s

15 μ s

15 μ s

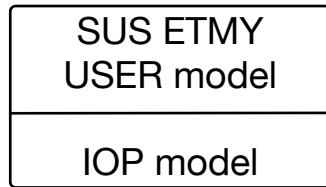
15 μ s

7.5 + 7.5 μ s

13 μ s light travel delay
-12 μ s single pole correction

61 μ s

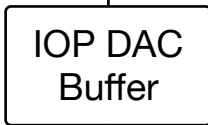
OMC Computation
Completes, control signal makes the IPC jump to the ends, and is received within the same clock cycle as SUSEM computation, so no extra 61 μ s is needed because there is no 16k clock cycle delay (see pg 6 of G1501195)



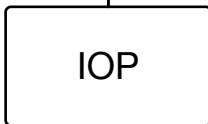
L3_LOCK_L_EXC
L3_LOCK_L_IN2

T = 0

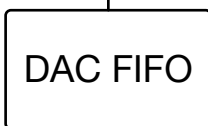
T = +61 μ s



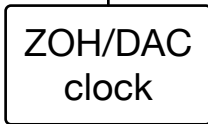
T = +76 μ s



T = +91 μ s



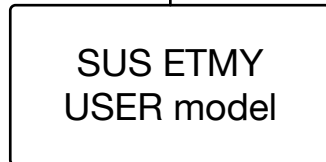
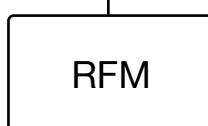
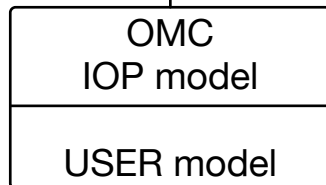
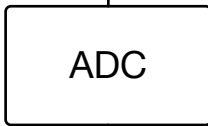
T = +106 μ s



T = +122 μ s



T = +123 μ s



T = +184 μ s

L3_LOCK_L_IN1